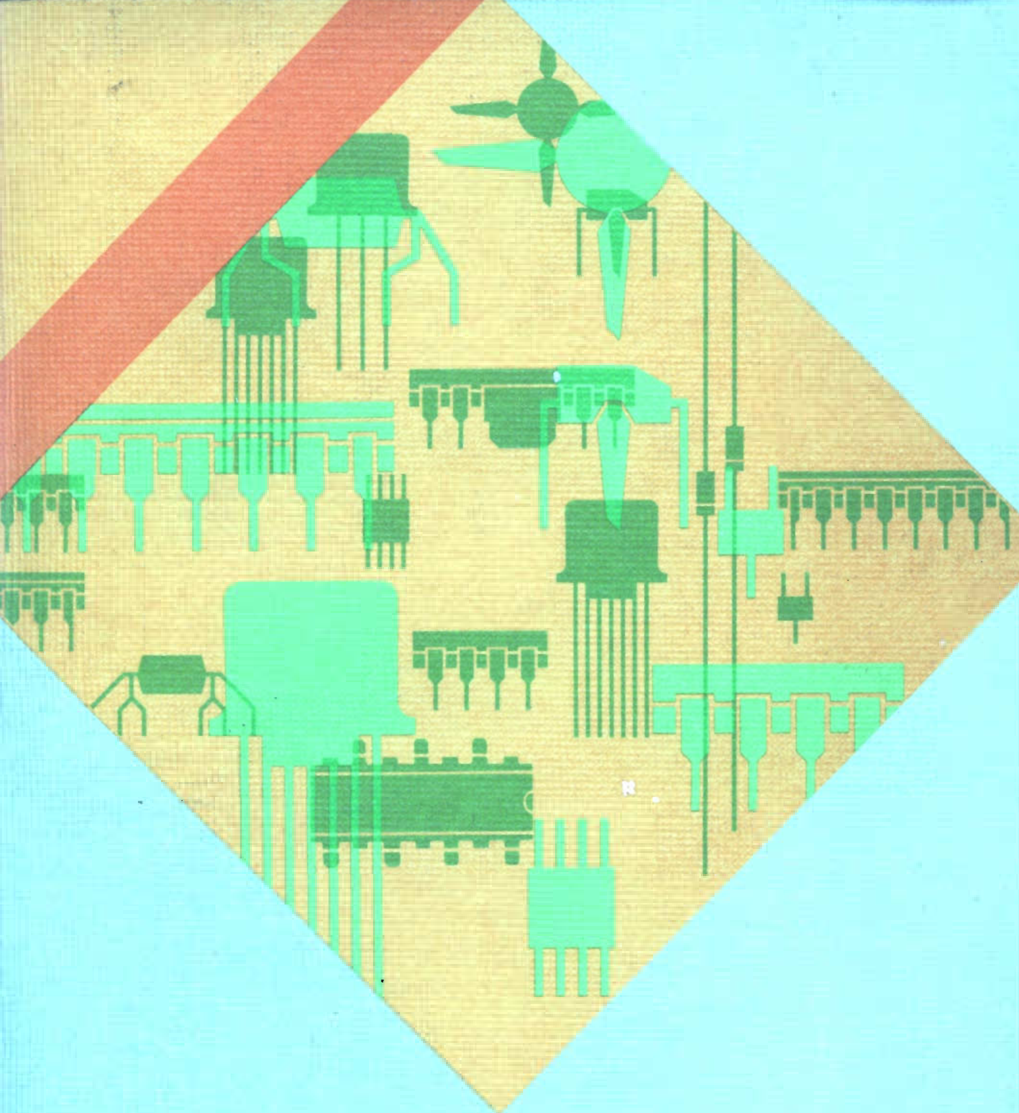

Integrated Circuits for Consumer Applications 1977/78

6250-09-1E

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ICs for Television and Radio Receivers

ICs for Electronic Clocks

ICs for Motor Vehicles

ICs for Electronic Organs

ICs for Other Applications

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Integrated Circuits for Consumer Applications

Manual 1977 / 78

Contents

	Page
General Information	7
Alphabetic Index of Types	9
Summary of Types	10
Technical Information	12
ICs for Television and Radio Receivers	19
ICs for Electronic Clocks	119
ICs for Motor Vehicles	133
ICs for Electronic Organs	145
ICs for Other Applications	165

General Information

Types	Page
SAA 1004-N	146
SAA 1005	150
SAA 1005-P	154
SAA 1008	20
SAA 1020	28
SAA 1021	28
SAA 1024	40
SAA 1025	44
SAA 1130	54
SAH 215	166
SAJ 110	158
SAJ 300 R	120
SAJ 300 T	122
SAK 215	134
SAY 115	138
TAA 550	190
TAA 780	124
TAA 790	66
TBA 800 C	72
TBA 940	80
TBA 950	86
TBA 950 : F	86
TCA 350 Y	170
TCA 380	176
TCA 700 X	142
TCA 720	94
TCA 860	128
TDA 0470-D	162
TDA 1035	96
TDA 1044	102
TDA 1044 F	102
TDA 1053	110
TDA 9400	112
TDA 9500	112

Types	Page
TDD 1605	180
TDD 1606	180
TDD 1608	180
TDD 1610	180
TDD 1612	180
TDD 1615	180
TDD 1618	180
TDD 1624	180
UAA 210	182
ZTE 1,5	186
ZTE 2	186
ZTE 2,4	186
ZTE 2,7	186
ZTE 3	186
ZTE 3,3	186
ZTE 3,6	186
ZTE 3,9	186
ZTE 4,3	186
ZTE 4,7	186
ZTE 5,1	186
ZTK 6,8	190
ZTK 9	190
ZTK 11	190
ZTK 18	190
ZTK 22	190
ZTK 27	190
ZTK 33	190

ICs for Television and Radio Receivers

SAA 1008	TV Character Generator
SAA 1020	IC Set for Controlling TV Tuners (Storage IC)
SAA 1021	IC Set for Controlling TV Tuners (Control IC)
SAA 1024	Thirty Channel Ultrasonic Transmitter for Remote-Controlled TV Receivers
SAA 1025	Thirty Channel Ultrasonic Receiver for Remote-Controlled TV Receivers
SAA 1130	Thirty Channel Ultrasonic Receiver with Program Store
TAA 790	Controlled Pulse Generator
TBA 800 C	5 W Audio Power Amplifier
TBA 940	Controlled Pulse Generator for Thyristor Line Output Stages
TBA 950	Controlled Pulse Generator for Transistor Line Output Stages
TBA 950:F	Controlled Pulse Generator for Transistor Line Output Stages in Multistandard TV Receivers
TCA 720	DC Converter
TDA 1035	Sound Channel IC for TV Receivers
TDA 1044	Frame Scan Circuit for TV Receivers
TDA 1053	PIN Diode π Network
TDA 9400	Line Circuit for TV Receivers with Thyristor Line Output Stage
TDA 9500	Line Circuit for TV Receivers with Transistor Line Output Stage

ICs for Electronic Clocks

SAJ 300 R	CMOS Circuit for RF Quartz Clocks with Digital Adjustment and 0.5 Hz Output
SAJ 300 T	CMOS Circuit for RF Quartz Clocks with Digital Adjustment and 64 Hz Output
TAA 780	1.1 V Stabilizing Circuit
TCA 860	Driving Circuit for Clocks with Single Coil Balance Systems

ICs for Motor Vehicles

SAK 215	Pulse Shaper for Revolution Counters
SAY 115	Speedometer and Mileage Indicator
TCA 700 X	Car Voltage Stabilizer

ICs for Electronic Organs

SAA 1004-N	Seven Stage Frequency Divider in I^2L Technique
SAA 1005	Seven Stage Frequency Divider in I^2L Technique
SAA 1005-P	Seven Stage Frequency Divider in I^2L Technique
SAJ 110	Seven Stage Frequency Divider
TDA 0470-D	Gate for Electronic Organs

ICs for Other Applications

SAH 215	Telephone Push-Button IC
TAA 550	Temperature-Compensated Stabilizing Circuit
TCA 350 Y	Delay Line for Analogue Signals
TCA 380	Duplex RF Delay Line
TDD 1605 . . . TDD 1624	Voltage Stabilizers for 5 . . . 24 V
UAA 210	Exposuremeter-IC
ZTE 1.5 . . . 5.1	Parallel Stabilizing Circuits
ZTK 6.8 . . . ZTK 33	Temperature-Compensated Stabilizing Circuits

Characteristics and Maximum Ratings, Recommended Operating Conditions

The electrical performance of a semiconductor device is usually expressed in terms of its characteristics and maximum ratings.

Characteristics are those properties of the device which can be measured by use of suitable measuring instruments and set-ups, and provide information on the performance of the device under specified operating conditions (at a given bias, for example). Depending on requirements, they are quoted either as typical values, guaranteed values or maximum ratings.

Typical values are expressed as figures or as one or more curves, and are subject to spreads.

Guaranteed values are preceded either by the symbol > (greater than) or < (less than); sometimes the guaranteed spread limits are indicated by two numbers with three dots between them. Occasionally a typical curve is accompanied by another curve, this being a 95 %, or, in a few cases, a maximum spread limit curve.

Maximum ratings give the values which cannot be exceeded without risk of damage to the device. Changes in supply voltage and in the tolerances of other components in the circuit must be taken into consideration. No single limit should ever be exceeded, even when the device is operated well within the other maximum limits. The inclusion of the word "admissible" in a title means that the associated curve defines the maximum ratings. If characteristics and maximum ratings are listed together without a separate heading, then the maximum ratings are identified by the word "admissible".

Because the performance of complex devices such as the ICs listed in this book cannot always be fully described in terms of characteristics and maximum ratings, it is sometimes necessary to describe some performance features by reference to a test circuit, which in many instances is the same as the recommended operational circuit. For some ICs, therefore, a third set of data is included under the heading "Recommended Operating Conditions".

Logic Levels

The logic levels of digital circuits are denoted by the letters "H" (high = maximum positive level) and "L" (low = minimum positive level). If positive logic is used, as usual in connection with bipolar ICs, "H" corresponds to logic "1" and "L" to logic "0".

In connection with MOS circuits the electrical states sometimes are denoted by negative logic, then the state "H" corresponds to logic "0" and "L" to logic "1".

Electrical Designations

The subscripts used in conjunction with the numerous electrical IC data (V - voltage, I - current, R - resistance, f - frequency, etc.) usually denote the associated lead numbers.

If a one-number subscript is used in conjunction with a voltage (V), then this means that the voltage is referred to circuit ground (usually - V_B, 0 V). When a two-number subscript is used, the voltage concerned is that measured between the two terminals, the terminal denoted by the first number usually being positive with respect to the other. Since a dual in line package has 14 pins, the subscript numbers are usually separated by diagonal strokes to reduce the risk of error. A "0" in the third place means, as with transistors, that the other pins of the device are open circuit.

Usually only a single-number subscript is used in conjunction with current. A current indicated as positive is assumed to flow into the pin concerned unless otherwise indicated by arrows on the associated circuit diagram.

Resistors, capacitors and inductors are normally numbered consecutively (e. g. $R1$, $R2$, etc.). If there are two numbers in the subscript (e. g. $R_{14/3}$), then this means that the resistor is connected between correspondingly numbered pins of the circuit.

Assembly Instructions

1. Plastic Encapsulation 50 B 4

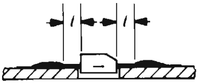
a) Devices with vertical pins (suffix "A").

These ICs can be soldered to printed circuit boards so that the bottom of the package rests flat on the side of the board opposite to that carrying the copper conductors.

The pins can be either dip- or hand-soldered. At a soldering temperature of 230 . . . 260 °C the soldering time must not exceed 7 sec.

b) Devices with horizontal pins (suffix "B")

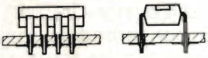
These ICs can be soldered to printed circuit boards so that the pins lie flat against the copper conductors with the plastic case projecting into a cut-out in the board.



Hand-soldering must be used. If the soldered joints are spaced more than 1.5 mm (dimension "l") from the case and a soldering temperature of 250 °C is used, then the soldering time must not exceed 8 sec.

2. Plastic TO-116 Encapsulation and similar

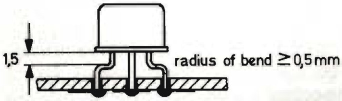
As shown in the figure below, the device is fitted to the component side of the board, the pins being soldered to the conductors on the opposite side. A shoulder on each lead ensures that the device cannot be pressed flat against the printed circuit board.



If hand- or dip-soldering at a temperature of 250 °C is used, the soldering time must not exceed 7 sec.

3. Metal Encapsulation similar to TO-5 with 6 to 14 leads

These devices may be mounted in any position. The leads must be bent not less than 1.5 mm from the bottom of the case and then splayed out in accordance with the grid dimensions.



The leads must be cut to the required length prior to the soldering process, which may be performed either by hand- or dip-soldering. The following solder times t_{max} in accordance with the solder temperatures mus be observed.

For dip-soldering:
t_{max} = 5 sec at 250 °C solder-bath temperature and
t_{max} = 4 sec at 300 °C solder-bath temperature.

For hand-soldering:
t_{max} = 15 sec with a soldering-iron temperature of 250 °C
t_{max} = 12 sec with a soldering-iron temperature of 300 °C
t_{max} = 8 sec with a soldering-iron temperature of 350 °C

If MOS components are soldered the soldering temperature should never exceed 300 °C. The solder-bath or soldering-iron and the printed board to be soldered should be kept at the same potential in order to avoid any harmful current flow. It is therefore recommended that the solder-bath or soldering-iron and the leads to be soldered be grounded.

4. Glass Encapsulation DO-35

At a recommended soldering temperature of ≤ 245 °C the maximum permissible soldering time must not exceed 5 sec. The minimum distance between case and solder point should be at least 4 mm when the component is mounted axis parallel to the p. c. board and 1.5 mm when mounted axis perpendicular to the p. c. board.

Protective Measures for MOS Components

In order to avoid destruction of the components by static discharges or noise voltages, protective structures have been provided at the inputs and outputs. They consist of PN junctions to the substrate which operate in the forward direction in the case of positive voltages; in the case of negative voltages they present a defined non-destructive breakdown. In this case integrated resistors limit the current. Furthermore, in the case of a negative voltage of about −40 V, a field-effect transistor at the input becomes conductive. For higher negative voltages this field-effect transistor constitutes a short-circuit.

All these protective measures behave as RC-networks; their component values depend upon the designed operating speed of the circuit.

If MOS components are not handled in the right way, it can easily happen that static discharges of some thousands of volts from capacitances of over 100 pF reach the connection pins. Despite the above-mentioned protective structures it is suggested therefore that the following recommendations be followed: The floor, the work-benches and the chairs should be provided with a conductive layer. Only metallic transport boxes should be used.

All tools which come into contact with the connection pins (test equipment, soldering-irons, flow-soldering equipment) should be at the same potential as the MOS circuits. Voltage peaks arising from switching operations should be carefully avoided.

MOS components should remain in their original packing (e. g. conductive foam) as long as possible. Before touching MOS components, the packing or the metal container should be touched in order to equalize potentials. Before inserting MOS circuits into printed boards it is imperative to touch the printed board first. MOS circuits should be the last components to be inserted into the printed board and soldered there. The connections of the printed board should remain short circuited until the board is finally used. MOS components must not be inserted or removed from the p. c. board if supply voltage is switched on.

Following these instructions is particularly important in those cases where persons handling MOS circuits wear clothes made from synthetic fibres or wool, or where they wear shoes with non-conductive soles.

Heat Removal from Integrated Circuits

The operation of any integrated circuit involves the dissipation of power with a consequent rise in junction temperature. Because the maximum admissible junction temperature must not be exceeded, careful circuit design with due regard not only to the electrical, but also the thermal performance of a semiconductor circuit, it essential.

If the dissipated power is low, then sufficient heat is radiated from the pins and from the surface of the case; if the dissipation is high, however, additional steps may have to be taken to promote this process by reducing the thermal resistance between the junction and the ambient air. This can be achieved either by pushing a star- or flag-shaped heat dissipator over the case, or by bolting the integrated circuit to a heat sink, or by soldering the pins and the cooling tabs to the copper foil of the p. c. board.

P, the power to be dissipated, T_j the junction temperature, and T_{amb}, the ambient temperature are related by the formula

$$P = \frac{T_j - T_{amb}}{R_{thA}} = \frac{T_j - T_{amb}}{R_{thC} + R_{thS}},$$

where R_{thA} is the total thermal resistance between junction and ambient air. The total thermal resistance in turn comprises an internal thermal resistance R_{thC} between the junction and the mounting base, and an outer thermal resistance R_{thS} between the case and the surrounding air (or any other cooling medium). It should be noted that only the outer thermal resistance is affected by the design of the heat sink. To determine the size of the heat sink required to meet given operating conditions, proceed as follows: First calculate the outer thermal resistance by use of the formula

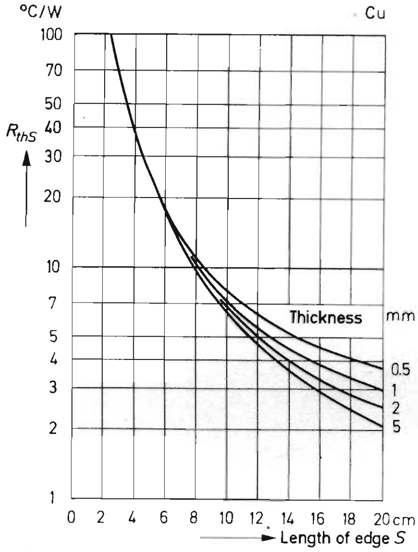
$$R_{thS} < \frac{T_j - T_{amb}}{P} - R_{thC}$$

and then, by the use of the diagrams shown on next page, determine the size of the heat sink which provides the calculated R_{thS}-value. To determine the maximum admissible device dissipation and ambient temperature limit for a given heat sink, proceed in the reverse order to that described above.

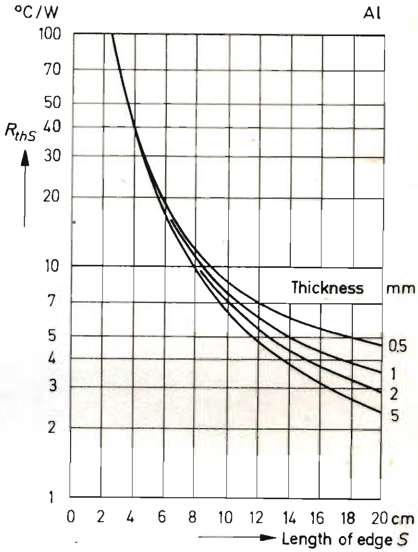
The calculations are based on the following assumptions: Use of a square-shaped heat sink without any finish, mounted in a vertical position; semiconductor device located in the centre of the sink; heat sink operated in still air and not subjected to any additional heat radiation. The calculated area should be increased by a factor of 1.3 if the sink is mounted horizontally, and can be reduced by a factor of approximately 0.7 if a black finish is used.

The curves on the following page give the thermal to ambient resistance of square vertical heat sinks as a function of side lenght. It is assumed that the heat is applied at the centre of the square.

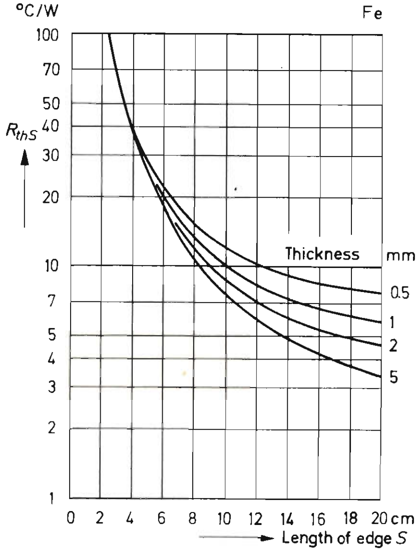
Copper Cooling Fin



Aluminium Cooling Fin



Steel Cooling Fin



ICs for Television and Radio Receivers

TV Character Generator

The SAA 1008 is a monolithic integrated MOS circuit in silicon gate technique for displaying a program number (1 . . . 16) on the screen of the television receiver, especially in combination with the INTERMETALL ultrasonic remote control receiver SAA 1130.

The fading-in of the program number occurs automatically on the following occasions: with every program command, with the recall command Z1, and with the command "Sequential program change" (see SAA 1130). The duration of the display is determined by an *RC* network. The numbers are displayed, within a darkened field constituted by 7 x 9 (4 x 9) dots, in the shape of a 5 x 7 dot matrix (ones) or a 2 x 7 dot matrix (tens). Each dot is approximately square and consists of six line sections equivalent to approximately 0.45 μs. The field area commences at a distance of 114 lines from the upper edge of the picture area and a distance of approximately 86 dots (two-digit number) or 90 dots (one-digit number) from the left margin of the picture. The formation of numbers by the 5 x 7 or 2 x 7 dot matrix can be adapted to comply with customer's wishes by varying the mask. By using appropriate external circuitry it would also be possible to display colored numbers on a field of different color.

The SAA 1008 is capable of processing signals from the ultrasonic remote-control receiver SAA 1130 directly. The control terminals of the SAA 1130 (pins 8 . . . 12) are connected to the control terminals of the SAA 1008: the SAA 1008 recognises the program command and the recall command Z1 (see table 1) from the 5-bit word supplied by the SAA 1130. The program outputs of the SAA 1130 are connected to the program inputs of the SAA 1008, and the SAA 1008 recognises the program number from the 4-bit word supplied by the SAA 1130 (see table 2).

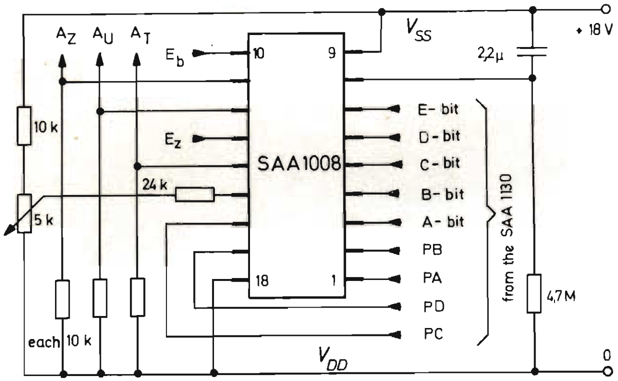
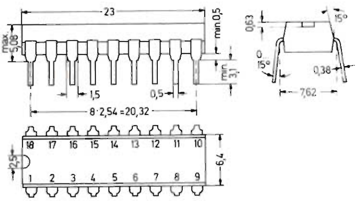


Fig. 1: Operating circuit of the SAA 1008

Fig. 2:
SAA 1008 in plastic package
20 A 18 according to DIN 41 866

Weight approximately 1.2 g
Dimensions in mm



Pin connections

1	Program input PA	10	Input E_b for vert. flyback pulse
2	Program input PB	11	Character output A_Z
3	Control input A-bit	12	Field-darkening output A_U
4	Control input B-bit	13	Input E_z for line flyback pulse
5	Control input C-bit	14	Clock frequency output A_T
6	Control input D-bit	15	Adjustment input E_p
7	Control input E-bit	16	Program input PC
8	Timing input E_K	17	Program input PD
9	Ground, 0, V_{SS}	18	Supply voltage V_{DD}

All voltages are referred to pin 9 *(V_{SS})*.

Maximum Ratings

Drain voltage	$-V_{DD}$	20	V
Voltage at the other pins	V_n	– 30 . . . +0.3	V
Drain currents, pins 11, 12 and 14	$-I_D$	5	mA
Ambient operating temperature range	T_{amb}	– 20 . . . +65	°C
Storage temperature range	T_S	– 55 . . . +125	°C

Recommended Operating Conditions

Supply voltage	$-V_{DD}$	18 (16.5 . . . 19.5)	V
Input voltages at pins 3 . . . 7	$-V_{IH}$	< 0.8	V
	$-V_{IL}$	> 4	V
Input voltages at pins 1, 2, 10, 13, 16 and 17	$-V_{IH}$	< 0.8	V
	$-V_{IL}$	> 6	V
Frequency of the internal clock oscillator	f_t	2.2	MHz
Pulse duration of signal E_b	t_b	0.2 . . . 1	ms
Pulse duration of signal E_z	t_z	4 . . . 12	µs

Characteristics at $-V_{DD}$ = 18 V, T_{amb} = 25 °C

Voltage drop across the output transistors at $-I_O$ = 1 mA	ΔV	< 1	V
Current consumption	$-I_{DD}$	28	mA

The table 1 has been taken from the SAA 1130 data sheet and shows the relationship between the commands and the output code at pins 8 . . . 12 of the SAA 1130. An additional column indicates which of the 31 commands in the SAA 1008 triggers the fading-in of the program number. The other commands do not affect the SAA 1008.

Table 1: Commands and outpout code of the SAA 1130, and their recognition by the SAA 1008

Command	Output code SAA 1130 at pins 8 . . . 12					
	E	A	B	C	D	
Sequential progr. change	L	H	H	H	H	recognised
Mains Off	H	L	H	H	H	
Sound Off	L	L	H	H	H	
Color saturation +	H	H	L	H	H	
Normalisation	L	H	L	H	H	
Color saturation –	H	L	L	H	H	
Additional command Z1	L	L	L	H	H	recognised
Brightness +	H	H	H	L	H	
Additional command Z2	L	H	H	L	H	
Brightness –	H	L	H	L	H	
Additional command Z3	L	L	H	L	H	
Volume +	H	H	L	L	H	
Additional command Z4	L	H	L	L	H	
Volume –	H	L	L	L	H	
Additional command Z5	L	L	L	L	H	
Program 1	H	H	H	H	L	
Program 2	L	H	H	H	L	
Program 3	H	L	H	H	L	
Program 4	L	L	H	H	L	
Program 5	H	H	L	H	L	
Program 6	L	H	L	H	L	
Program 7	H	L	L	H	L	
Program 8	L	L	L	H	L	recognised (Program 1 . . . 16)
Program 9	H	H	H	L	H	
Program 10	L	H	H	L	L	
Program 11	H	L	H	L	L	
Program 12	L	L	H	L	L	
Program 13	H	H	L	L	L	
Program 14	L	H	L	L	L	
Program 15	H	L	L	L	L	
Program 16	L	L	L	L	L	

Table 2 below has also been taken from the SAA 1130 data sheet. It shows the code in which information on the selected program is delivered at pins 6, 7, 13 and 14 of the SAA 1130. The table also applies to the program inputs of the SAA 1008, i. e. the pins 1, 2, 16 and 17.

Table 2: Output code of the SAA 1130 program outputs and input code of the SAA 1008 program inputs

Program number	Code PA	PB	PC	PD
1	L	L	L	L
2	H	L	L	L
3	L	H	L	L
4	H	H	L	L
5	L	L	H	L
6	H	L	H	L
7	L	H	H	L
8	H	H	H	L
9	L	L	L	H
10	H	L	L	H
11	L	H	L	H
12	H	H	L	H
13	L	L	H	H
14	H	L	H	H
15	L	H	H	H
16	H	H	H	H

Design and Operation Mode of the SAA 1008

The function of the SAA 1008 will be explained with reference to the various pins.

Pins 1, 2, 16 and 17 – program inputs PA . . . PD
To these inputs, information on the selected program must be statically applied in binary-coded form. The required code is shown in table 2. This coded signal is preferably taken directly from the program outputs of the SAA 1130.

Pins 3 . . . 7 – A-bit . . . E-bit control inputs
By means of the signal applied to these inputs, which is to be coded according to table 1 and supplied preferably directly from the control terminals of the SAA 1130, the fading-in of the program number on the screen of the TV receiver can be triggered. As table 1 shows, the program number display occurs with every program command, with the command "Sequential program change" and with the additional command Z1. What is being displayed in each case is the program number statically applied in coded form to the program inputs.

Pin 8 – timing input E_K
An *RC* network is connected to this pin, its time constant determining the duration of the program number display. The display is triggered by briefly connecting pin 8 to V_{SS}. The values entered in Fig. 1 for this *RC* network result in a duration of approximately 2 seconds.

Pin 9 – ground, 0, V_{SS}
Positive terminal of the supply voltage, substrate, reference potential. All voltage levels are related to this potential.

Pin 10 – input E_b for the vertical flyback pulse
To this pin is to be applied the vertical flyback pulse in a shape shown in Fig. 3.

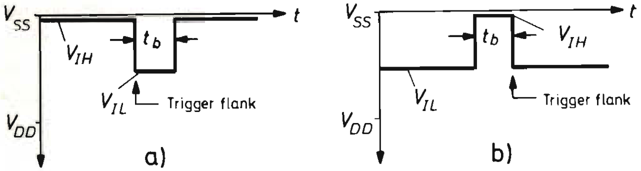


Fig. 3: Shape of the input signal at pin 10
a) for negative-going pulses
b) for positive-going pulses

Pin 11 – character output A_Z
Output supplying character information. Drain terminal of an open-drain transistor. The output signal shown in Fig. 4 is obtained if a load resistance is connected between pin 11 an V_{DD} (see Fig. 1). It applies to the first line composing the number "15".

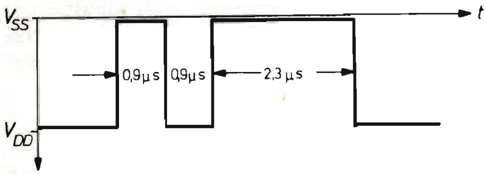


Fig. 4: Shape of the output signal at pin 11

Pin 12 – field-darkening output A_U
Output for the field-darkening operation. Drain terminal of an open-drain transistor. The output signal shown in Fig. 5 is obtained if a load resistance is connected between pin 12 and V_{DD} (see Fig. 1).

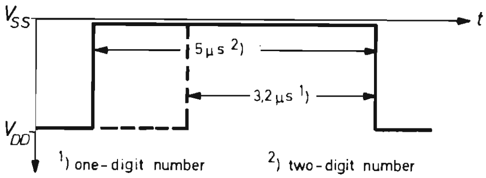


Fig. 5: Shape of the output signal at pin 12

Pin 13 – input E_z for the line flyback pulse
To this pin is to be applied the line flyback pulse in a shape shown in Fig. 6.

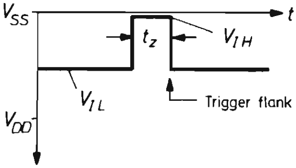


Fig. 6: Shape of the input signal at pin 13

Pin 14 – clock frequency output A_T
For measuring purposes, the signal of the internal clock oscillator is required externally. In normal operation this is not the case. Pin 14 is then left vacant.

Pin 15 – adjustment input E_p
For the fine adjustment of the clock frequency, a variable direct voltage is applied to this input which is preferably obtained by means of the supply voltage potential divider shown in Fig. 1. The clock frequency determines the dot width within characters to be displayed, and the distance of the display field from the left-hand edge of the frame. Its nominal value is 2.2 MHz. If it is to be set with the aid of a frequency meter, pin 13 must be connected to V_{DD} during the trimming operation.

Pin 18 – supply voltage V_{DD}
Negative terminal of the supply voltage; in television receivers, usually connected to ground.

Block Diagram of the SAA 1008

Fig. 7 shows a simplified block diagram of the SAA 1008. The frequency of the adjustable integrated oscillator (2.2 MHz) is applied to two clock generators which derive from it a two-phase clock of 2.2 MHz and 314 kHz (2.2 MHz : 7). At output A_T it is possible to measure the oscillator frequency if this terminal is connected to V_{DD} through a pull-up resistor. During the frequency measurement it is also necessary to connect input E_z to V_{DD}.

The input tester examines the 5-bit word supplied by the SAA 1130 to the control inputs A . . . E and evaluates the combinations listed in table 1 as commands for fading-in the program number. The number displayed is determined by the 4-bit combination applied to the program inputs (see table 2). The appropriate number is called up in the number memory via a decoder. Data for each line are read out serially, the position of the faded-in number on the screen being determined by the X-counter and the Y-counter.

The duration of the display is determined by the integrated timer in connection with the externally connected *RC* network at pin 8 (see Fig. 1).

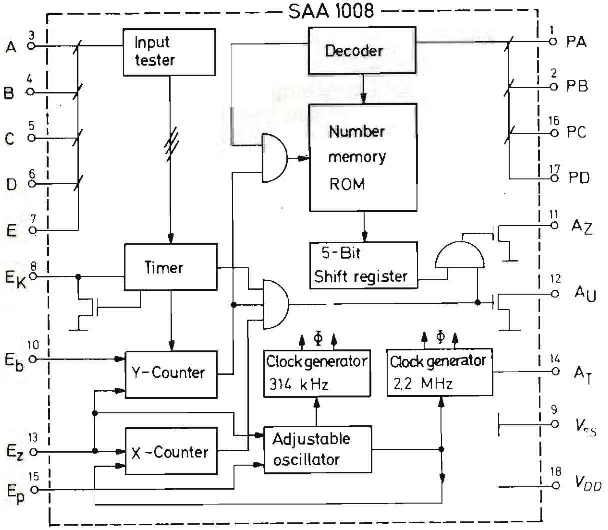


Fig. 7: Block diagram of the SAA 1008

IC Set for Controlling TV Tuners

This IC set consists of two integrated MOS circuits. The storage IC functions as a static shift register and has an extremely low current consumption. The control IC SAA 1021 performs the data processing duties. This IC set generates digitally and electronically all the data required for tuner control such as the tuning voltage, the switching voltage for band selection and an additional fine-tuning signal. Realisation of electronic station searching with silent tuning is possible.

In conjunction with with INTERMETALL's ultrasonic remote control system, transmitter SAA 1024 and receiver SAA 1130, and also with the character display circuit – all of which fully compatible with each other – an optimum overall solution has now been achieved to the design complex "remote control, electronic touch-buttons, channel storage, tuner control and program number display in modern color television receivers". The block diagram of Fig. 1 illustrates the interconnection of the ultrasonic receiver IC SAA 1130 to the IC set SAA 1020/SAA 1021 for the tuner control into on complete remote-control and channel selection operating unit.

The designer of a TV set which is equipped with the ICs SAA 1020/SAA 1021 has two possibilities concerning automatic station search and fine tuning. Hereafter, these two possibilities are called Option I and Option II. They are selected by different connection of pin 23 of the SAA 1021.

Option I:
The TV set can be programmed by an automatic station search operation. Stop signals for interrupting the search operation may be delivered i. e. by the ratio detector of the AFC. During normal TV operation fine-tuning may be adjusted in seven steps, even remote-controlled. The fine-tuning

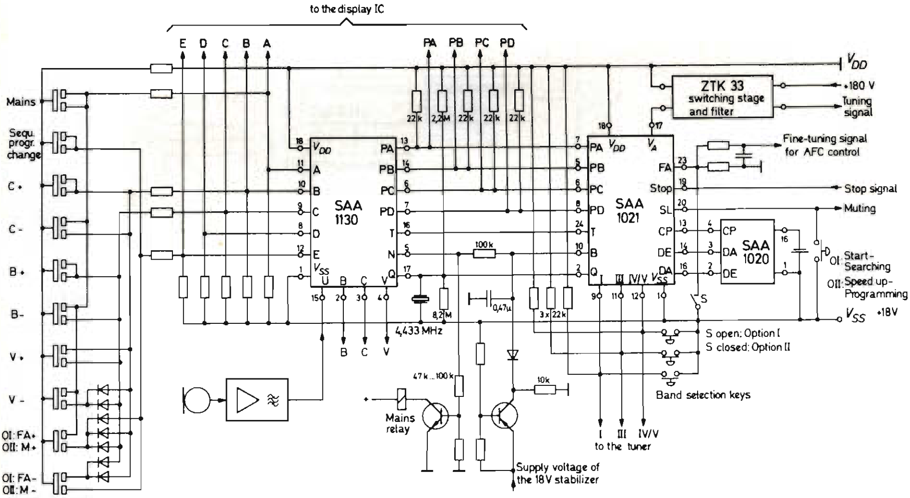


Fig. 1: Control assembly for a remote-controlled color TV receiver

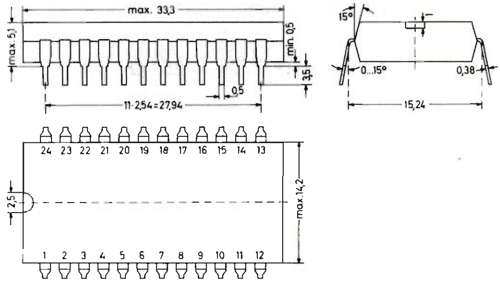
signal may serve as a guide signal for the AFC or it can be superimposed to the basic tuning signal. With that the user of the TV set either can alter the picture sharpness or compensate interferences at weak received stations.

Option II:
In this case the TV set is programmed by a manual station search operation. This is possible with two different speeds and in single steps. The slower speed and the single steps are also remote-controllable. Therefore, a remote-controlled picture correction is also possible, but a fine-tuning signal is not yet disposable. Ratio detector or AFC respectively are not necessary. For this operation mode the fine-tuning output pin 23 must be connected to V_{SS}.

Control IC SAA 1021

Monolithic integrated circuit in silicon gate technique

Fig. 2: SAA 1021 in plastic package 20 B 24 according to DIN 41 866
Weight approximately 3.5 g   Dimensions in mm



Pin connections

1	IC substrate, V_{SS}	16	Data output DA
2	Quartz terminal Q	17	Tuning voltage V_A
3	NC	18	Supply voltage V_{DD}
4	Leave vacant	19	Stop input
5	Program input PB	20	Option I: Start searching for stations
6	Program input PC		Option II: Speed up programming operation
7	Program input PA	21	Clock output GC
8	Program input PD	22	Leave vacant
9	Input/output band I	23	Option I: Fine tuning voltage FA
10	Blocking input B		Option II: Option switch-over signal
11	Input/output band III	24	Control input T
12	Input/output band IV/V		
13	Storage clock output CP		
14	Data input DE		
15	Leave vacant		

All voltages are referred to pin 1 (V_{SS}).

Maximum Ratings

Drain voltage	$-V_{DD}$	20	V
Voltage at the other pins	V_n	$-30\ldots+0.3$	V
Output currents	$-I_D$	5	mA
Ambient operating temperature range	T_{amb}	$-20\ldots+65$	°C
Storage temperature range	T_S	$-55\ldots+125$	°C

Recommended Operating Conditions

Supply voltage	$-V_{DD}$	18 (16.5 . . . 19.5)	V
Input voltages at pins 5 . . . 12, 14, 19, 20 and 24			
High-state	$-V_{IH}$	≤ 0.8	V
Low-state	$-V_{IL}$	≥ 6	V
Quartz-controlled clock frequency at pin 2	f_t	4.4336	MHz

Characteristics at $-V_{DD} = 18$ V, $f_t = 4.4336$ MHz, $T_{amb} = 25$ °C

Current consumption	$-I_{DD}$	32	mA
Voltage drop across the output transistors at $-I_D = 1$ mA, pins 9 . . . 12, 17, 19, 20 and 23	ΔV	< 0.6	V
Output frequency pins 21 and 23	f_{FA}	19 793	Hz
Pulse duty factor of the output signal at pin 21 (pulse ≙ high state)	t_p/t_0	6 : 1	
Pulse duty factor of the output signal at pin 23 (pulse ≙ high state)	t_p/t_0	6 : 1 . . . 0 : 7	
Storage clock output CP (pin 13) with transistor on the V_{SS} side conducting, at $-I_{13} = 1$ mA	ΔV_{13}	< 0.4	V
with transistor on the V_{DD} side conducting, at $R_{13/1} = 1.2$ kΩ	$-V_{13}$	> 2	V
Data output DA (pin 16) with transistor on the V_{SS} side conducting, at $-I_{16} = 0.2$ mA	ΔV_{16}	< 0.4	V
with transistor on the V_{DD} side conducting, at $R_{16/1} = 6$ kΩ	$-V_{16}$	> 2	V

Design and Operation Mode of the SAA 1021
explained with reference to the various pins.

Pin 1 – IC substrate, V_{SS}
This pin must be connected to the positive terminal of the supply voltage. All voltage levels are related to the potential on this pin.

Pin 18 – Supply voltage V_{DD}
This pin must be connected to the negative terminal of the supply voltage V_{DD}.

Pin 2 – Quartz terminal Q
This input must be connected to the quartz terminal of the SAA 1130. Here, a quartz crystal including bias voltage divider should be connected if the SAA 1021 is operated without the SAA 1130.

Pin 17 – Tuning voltage V_A
This output issues the digital tuning information by means of which the tuning voltage for the variable capacitance diodes of the tuner is generated with the aid of a switching stage and an *RC* low-pass filter. The tuning voltage can be set in 3968 steps.

The modulation process is a modified pulse duration modulation whose repetition rate of the pulse pattern remains constant at 558.67 Hz (color sub-carrier frequency divided by 2 times 3968).

Given a tuning voltage rising from zero, we have as the minimum value at the output of the SAA 1021 a low-pulse of approximately 0.46 μs duration to begin with. This duration subsequently increases in 62 steps of 0.46 μs each up to approximately 28 μs. With the 63rd step appears at the output in each period a pulse of 28 μs duration and a second one of 0.46 μs duration, the latter again being enlarged step-wise up to 28 μs duration. This is followed by two 28 μs pulses and one pulse starting with 0.46 μs of step-wise encreased duration and so forth.

On the one hand, the advantage of this arrangement is that worst-case ripple in the output signal is reduced by the factor of approximately 16 in comparison with ordinary pulse duration modulation. On the other hand, compared with the rate multiplier principle, the number of rising and falling flanks per period is reduced by the factor 64. This excludes falsification of the tuning voltage by the switching flanks.

Pin 9, 11 and 12 – Band inputs/outputs
These three outputs supply data to the tuner and serve as inputs for manual band switching. They are connected to the drain terminals of open-drain output transistors and the transistor which conducts is always the one whose band has been switched on.

If, for example, in the case of new programming a channel key, the band is changed at the receiver's front panel, this is done by using the band selection key (Fig. 1) to connect the associated band output to V_{SS}. This information is at first stored in the SAA 1021 until it is taken over by the storage device SAA 1020 together with the tuning voltage data on completion of a station search upon actuation of a fine-tuning sensor plate (FT, Fig. 1).

The band data stored in the SAA 1021 will be rewritten if different band data are read from the storage IC SAA 1020, e. g. when the TV program is changed ultrasonically.

If a fourth band is required, e. g. for cable TV, the signal "all three band outputs blocked" may be introduced instead. For the purpose of manual band selection, all three band outputs must then be briefly connected to V_{SS}.

Pin 20, Option I – Start searching for stations
Programming the channel selection keys – an operation actually to be undertaken only when using the receiver for the first time – can only be carried out at the receiver itself and, in the case of a set designed according to Option I, takes place as follows:

First, a storage location is chosen by actuating a channel key. At this, band and tuning data stored by chance in the storage IC SAA 1020 are taken over into the control IC SAA 1021. Then, the band selection key is depressed which corresponds to the band in which the station to be stored is situated. The key "Start" is now depressed and pin 20 is thus briefly connected to V_{SS}. This initiates the automatic search operation. After this operation has been stopped by a final stop signal the band and tuning voltage data are automatically stored in the SAA 1020. The fine-tuning output is normalised during station searching operation.

If silent tuning (muting) is envisaged, the data required for this purpose can likewise be derived from pin 20. After the key "Start" is released, pin 20 is connected by means of an integrated transistor to V_{SS} potential for the duration of the search run. If, instead of the station responding first because it requires the lowest tuning voltage, the user wishes to select a different station, the key "Start" should be actuated once more which will cause the station with the next-higher tuning voltage to be stored and so forth.

Selecting a channel and start of the station searching operation may be fitted to one respective key via a diode matrix. The speed of the automatic station search run in the three bands is adapted to the slope of the tuner's voltage/frequency characteristic. The entire band IV/V is traversed in 14.2 seconds. In band III, five steps are comprised into a single step, so that the band is traversed within 2.84 seconds, while in band I ten steps are comprised into a single step, resulting in a traverse time of 1.42 seconds.

Pin 19 – Stop of station searching
This pin is used in Option I receivers only and serves as input for the stop signal in connection with an automatic station searching operation. In the non-operative condition, Low-potential must be applied to pin 19 (V_{DD}). The first stop signal briefly switches the pin 19 High (V_{SS}). The trailing edge of the stop signal (HL) changes the direction of the search run, and the leading edge (LH) of the subsequent second stop signal terminates the search. Since the tuning voltage, which is integrated by means of the *RC* lowpass filter becomes available after the digital information, the first stop signal appears too late, and the tuning voltage slightly overruns the station. Therefore, the stop signal is automatically followed by a correction run in the reverse sense which takes place with

a speed 20 times slower than the search run, so that the discrepancy between digital information and integrated tuning voltage upon a renewed stop amounts to less than half a step. The selected station is stored in the SAA 1020 not before this final stop signal becomes effective.

Stop signals may be derived from a ratio detector or a similar circuit.

Pin 20, Option II – Speed-up programming operation
In the case of a receiver designed according to Option II, the channel selection keys are programmed in the following manner: At first the relevant channel selection key is operated and then the band selection key. Thereafter, the search run is initiated in that the sensor plates M+ (manually forward) or M– (manually backward) are touched. Pin 20 connected to V_{SS} at the same time by depressing the key "Fast" will result in a rate of change of the digital output signal at pin 17 of 90 steps per second. By this means a channel intervall is traversed within two seconds, which enables the user to stop in good time. If the button "Fast" is not depressed, the tuning information varies at seven steps per second, so that fine tuning of the chosen station becomes possible.

When planning an Option II receiver, the designer can choose between various possibilities concerning the layout of the search run controls. The first alternative has been indicated in the description above. As a second alternative, four tuning keys should be provided, i. e. fast forward, slow forward, fast backward and slow backward. Even a four-function lever resembling a gear lever would be feasible.

The M+ and M– commands may be given by sensor plates on the receiver or ultrasonically (commands Z4 and Z5, see the SAA 1130 data sheet). If the M+ or M– plates are touched continuously, the digital tuning data at pin 17 are first varied by one step, and this is followed by a pause of about 0.6 seconds, whereupon further tuning steps are produced at intervals of about 0.14 seconds. Thus, three ways of varying the tuning voltage are feasible: a single step if the sensor plate is touched for a time under 0.6 seconds, slow variation by continuous touching of the sensor, and fast variation if the sensor M+ or M– and the button "Fast" are actuated simultaneously.

The rate of change of the tuning data is adapted to the slope of the tuner's voltage/frequency characteristic also in the Option II TV receiver in that five steps are comprised into one step in the case of band II, and ten steps into one step in the case of band I.

When used in an Option II receiver the IC set may also be programmed for semi-automatic station searching if an external auxiliary circuit ensures that a changeover from a fast rate of tuning data variation to a slow variation rate is triggered by some stop signal, e. g. derived from the synchronising circuit, when a receivable station synchronises deflection. In that case an automatic stop is obtained near the exact station setting, and fine tuning can be performed manually.

Pin 23 – Option I: Fine-tuning voltage FA
This output delivers fine-tuning information in the shape of a square wave voltage whose pulse duty factor is variable in seven steps and whose frequency amount to 19 793 Hz. The mean value of the square wave voltage is obtained by means of an *RC* network. The user of the

TV receiver can make fine-tuning adjustments manually, either by touching the sensor plates FA+ or FA– or, ultrasonically, by the commands Z4 and Z5. The pulse duty factor of the fine-tuning square wave voltage is variable between 6 : 1 and 0 : 7.

Manual fine-tuning enables the user to deviate from the automatic tuning. With it he can possibly adjust the picture to more sharpness or weakness in order to compensate unfavourable receiving conditions.

When the automatic station search is started by actuating the button "Start", the fine-tuning voltage is standardised – with a pulse duty factor of the output square wave voltage of 4 : 3 with a period approximately 50 µs.

After every fine-tuning step, the new information is immediately accepted by the storage device SAA 1020. If the same channel is selected at a later date, the stored fine-tuning level becomes effective again.

Pin 23 – Option II: Option switch-over signal
If this pin is taken to V_{SS} (indicated by the switch S in Fig. 1), then the IC set is programmed for the Option II operation mode.

Pin 24 – Control input T
This input receives control pulses from the SAA 1130. In the Option I mode the fine-tuning data can be altered with these pulses and in the Option II mode the tuning information. Tuning information in the forward direction is varied by pulses of approximately 22 µs duration and in the backward direction by pulses of about 22 ms duration. At that the speed is seven steps per second.

Pin 21 – Clock output GC
This output delivers a clock signal the frequency of which is approximately 20 kHz and the pulse duration (V_{DD}) about 7 µs. This signal is assigned for the control of non-volatile MNOS storage devices.

Pin 10 – Blocking input B
In an operating TV set this pin is switched to V_{SS} potential. By switching it to V_{DD} the SAA 1021 will be blocked internally and will not accept any commands for changing band or tuning data. The blocking input receives its control signal (100 kΩ resistor in Fig. 1) from the mains output (pin 5) of the SAA 1130. Thus the SAA 1021 becomes operative only if the mains flip-flop in the SAA 1130 is switched on. Additionally, pin 10 may be equipped with a PNP transistor stage which blocks the SAA 1021 at the correct instant and again releases it delayed only if a sufficient supply voltage is available. This stage in conjunction with the blocking input prevents execution of incomplete reading cycles resulting from an incorrect supply voltage caused by short breakdowns of the mains.

Pin 13 – Storage clock output CP
This push-pull output is low-ohmic and therefore the clock line is unsensitive against interferences. This output supplies 288 pulses at a frequency of 138 kHz to the storage IC SAA 1020 for every write or read cycle.

Pin 14 – Data input DE
Via this input the storage IC SAA 1020 supplies data to the SAA 1021.

Pin 16 – Data output DA
This output issues data to the SAA 1020. During any writing or reading cycle the shift register in the storage IC is connected in a closed loop via pins 14 and 16. The entire contents of the data store are circulated once and in each case one 18-bit word will be read or rewritten.

Pins 5 . . . 8 – Program inputs PA . . . PD
The program information will be supplied statically in binary-coded form by the program outputs of the SAA 1130. These outputs are directly connected to the program inputs of the SAA 1021. The table below shows the code. During a read or write cycle, this program information determines the address of the storage device SAA 1020.

Table 1: Input code for the programm inputs PA . . . PD of the SAA 1021

Program number	PA	PB	PC	PD
1	L	L	L	L
2	H	L	L	L
3	L	H	L	L
4	H	H	L	L
5	L	L	H	L
6	H	L	H	L
7	L	H	H	L
8	H	H	H	L
9	L	L	L	H
10	H	L	L	H
11	L	H	L	H
12	H	H	L	H
13	L	L	H	H
14	H	L	H	H
15	L	H	H	H
16	H	H	H	H

Block Diagram of the SAA 1021

Fig. 3 is a block diagram which shows the internal layout of the SAA 1021 and which will be explained in further detail.

The integrated oscillator controls a clock generator. It comprises essentially a 4-by-1 divider and an 8-by-1 divider, generating a 1 MHz and a 138 kHz two-phase clock. The 138 kHz clock signal has a pulse duty factor of 3 : 5. The faster clock signal clocks the tuning voltage generator and the slower one all the rest of the IC.

The signal generator which generates the tuning voltage at pin 17 consists of a special pulse duration modulator circuit. Its control logic circuit determines the rate of change of the tuning voltage in both operation modes. It recognises stop signals in Option I, generates the forward or backward commands in Option II (controlled by the input T), recognises

the start of the station search in Option II and the command "Fast" in Option II (both from pin 20).

The transfer logic effects connection to the storage IC SAA 1020 and consists mainly of a comparator and word counter. In the comparator, the static program address PA . . . PD is compared with the word counter information. In this way, the address of the 18-bit word in the 16 x 18 bit shift register SAA 1020 is established and becomes effective during a transmission.

The pulse duration measuring unit connected to the input T recognises the duration of the applied signal (approx. 20 μs or approx. 20 ms resp.). On the strength of this information, the fine tuning data are changed in Option I, and the direction in which the tuning information is varied is established in the Option II mode.

Any errors which may be caused in band switching by the simultaneous actuation of several band selection keys are suppressed by an error recognition circuit connected to pins 9, 11 and 12.

An internal blocking circuit which is connected to the external blocking circuit by an OR gate ensures that a read cycle is automatically initiated in order to call up the channel selected after the supply voltage V_{DD} has been switched on.

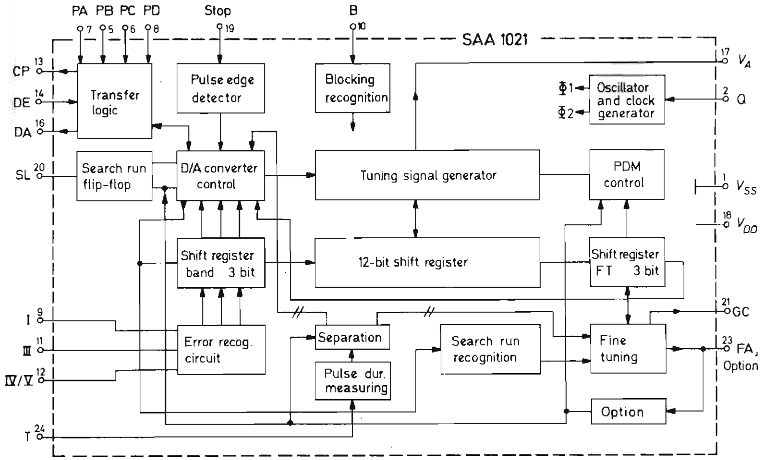


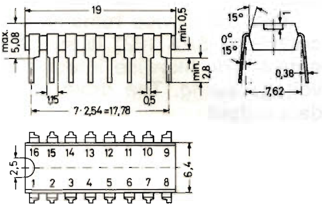
Fig. 3: Block diagram of the SAA 1021

Storage IC SAA 1020

Monolithic integrated circuit in CMOS technique

Fig. 4:
SAA 1020 in plastic package
20 A 16 according to DIN 41 866

Weight approximately 1.2 g
Dimensions in mm



Pin connections

1	Ground, V_{SS}, substrate	4	Clock input CP
2	Data input DE	5 . . . 15	NC
3	Data output DA	16	Supply voltage V_B

All voltages are referred to pin 1 (V_{SS}).

Maximum Ratings

Drain voltage	V_B	– 3.5 . . . +0.3	V
Input voltages	V_2, V_4	– 15 . . . +0.3	V
Output voltage	V_3	– 10	V
Ambient operating temperature range	T_{amb}	– 20 . . . +65	°C
Storage temperature range	T_S	– 55 . . . +125	°C

Recommended Operating Conditions

Supply voltage	$-V_B$	1.5 . . . 3	V
Clock frequency	f_t	140	kHz

Characteristics at $-V_B = 1.5$ V, $T_{amb} = 25$ °C

Non-operative current consumption	$-I_B$	10	µA
Operative current consumption	$-I_B$	100	µA
Input resistances	$R_{2/1}$	10	kΩ
	$R_{4/1}$	2	kΩ
Saturation current of the output transistor at $-V_B = 1.2$ V	I_3	$>$ 0.2	mA

Design and Operation Mode of the SAA 1020

The SAA 1020 is a static 288-bit shift register capable of storing 16 channel data. It can be directly connected to the control IC SAA 1021 without interface. The clock input is terminated with an integrated resistor $R_{4/1}$ so that the device remains insensitive also if the supply voltage of the control IC SAA 1021 is switched off and its push-pull output turns high-ohmic. The likewise integrated resistor $R_{2/1}$ at the data input limits the voltage swing. The drain connection of an open-drain transistor is the data output.

Thirty Channel Ultrasonic Transmitter for Remote-Controlled TV Receivers

Monolithic integrated circuit in CMOS technique. The SAA 1024 is intended for remote control systems whereby 30 commands are transmitted by means of 30 different ultrasonic frequencies. The SAA 1025, produced by INTERMETALL, is recommended as a suitable receiver.

The SAA 1024 comprises an oscillator circuit, a variable and a fixed frequency divider, a decoder and a command error protection. Fig. 1 shows the circuit diagram of an ultrasonic transmitter based on the SAA 1024.

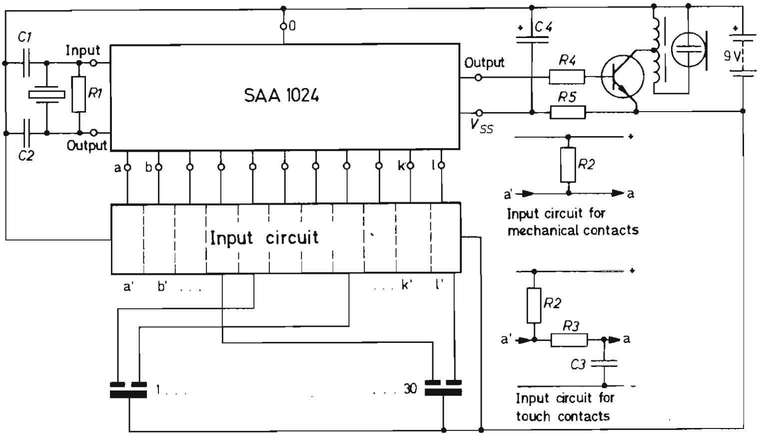
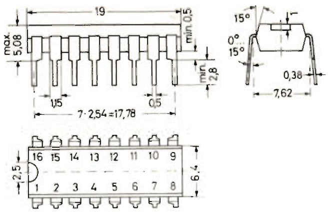


Fig. 1: Circuit diagram of an ultrasonic transmitter based on the SAA 1024

Fig. 2:
SAA 1024 in dual in-line plastic SOT-38 package
20 A 16 according to DIN 41 866

Weight approximately 1.2 g
Dimensions in mm



Pin connections

1	Oscillator input	9	Input g
2	Oscillator outpout	10	Input h
3	Input a	11	Input i
4	Input b	12	Input k
5	Input c	13	Input l
6	Input d	14	V_{SS}
7	Input e	15	Ultrasonic output
8	Input f	16	Ground, 0, substrate

All voltages are referred to pin 16.

Maximum Ratings

Supply voltage	V_{SS}	+ 0.3 . . . − 12	V
Voltage at the other pins	V_n	+ 0.3 . . . V_{SS}	
Output current	$\|I_{15}\|$	10	mA
Ambient operating temp. range	T_{amb}	− 10 . . . + 60	°C
Storage temperature range	T_S	− 30 . . . + 125	°C

Recommended Operating Conditions

Supply voltage	V_{SS}	− 7 . . . − 9	V
Oscillator frequency (colour sub-carrier)	f_t	4.4336	MHz
Capacitors (see Fig. 1)	$C1$	39	pF
	$C2$	47	pF
	$C3$	100	pF
	$C4$	47	µF
Resistors (see Fig. 1)	$R1$	10 (4.7 . . . 22)	MΩ
	$R2$	47	MΩ
	$R3$	1	MΩ
	$R4$	2.7	kΩ
	$R5$	47	Ω

Characteristics at $V_{SS} = -9$ V, $T_{amb} = 25$ °C

Ultrasonic output impedance High state at $I_{15} = -1$ mA	R_{OH}	500	Ω
Lowe state at $I_{15} = 0.2$ mA	R_{OL}	1.5	kΩ
Threshold voltage at inputs a . . . l	V_{in}	− 4.9	V
Voltage hysteresis at inputs a . . . l	ΔV_{in}	0.45	V
Input current at inputs a . . . l at $V_{in} = 0$ V . . . V_{SS}	$\|I_{in}\|$	10	nA
Current consumption with oscillator running, ultrasonic output open-circuit	I_{14}	− 2	mA
with oscillator quiescent	I_{14}	− 10	µA
Ultrasonic transmission frequencies at $f_t = 4.4336$ MHz	see table overleaf		

Table 1: Ultrasonic Transmission Frequencies at f_t = 4.4336 MHz

Key No.	Fre-quency	x	a	b	c	d	e	f	g	h	i	k	l
1	33 945 Hz	98	H	H	H	H	L	H	H	L	H	H	H
2	34 291 Hz	99	H	H	H	H	L	H	H	H	H	H	L
3	34 638 Hz	100	H	H	H	H	L	H	L	H	H	H	H
4	34 984 Hz	101	H	H	H	H	L	H	H	H	H	L	H
5	35 330 Hz	102	H	H	H	H	L	L	H	H	H	H	H
6	35 677 Hz	103	H	H	H	H	L	H	H	H	L	H	H
7	36 023 Hz	104	L	H	H	H	H	L	H	H	H	H	H
8	36 370 Hz	105	L	H	H	H	H	H	H	H	L	H	H
9	36 716 Hz	106	H	L	H	H	H	L	H	H	H	H	H
10	37 062 Hz	107	H	L	H	H	H	H	H	H	L	H	H
11	37 409 Hz	108	H	H	L	H	H	L	H	H	H	H	H
12	37 755 Hz	109	H	H	L	H	H	H	H	H	L	H	H
13	38 101 Hz	110	H	H	H	L	H	L	H	H	H	H	H
14	38 448 Hz	111	H	H	H	L	H	H	H	H	L	H	H
15	38 794 Hz	112	L	H	H	H	H	H	L	H	H	H	H
16	39 141 Hz	113	L	H	H	H	H	H	H	H	H	L	H
17	39 487 Hz	114	H	L	H	H	H	H	L	H	H	H	H
18	39 833 Hz	115	H	L	H	H	H	H	H	H	H	L	H
19	40 180 Hz	116	H	H	L	H	H	H	L	H	H	H	H
20	40 526 Hz	117	H	H	L	H	H	H	H	H	H	L	H
21	40 872 Hz	118	H	H	H	L	H	H	L	H	H	H	H
22	41 219 Hz	119	H	H	H	L	H	H	H	H	H	L	H
23	41 565 Hz	120	L	H	H	H	H	H	H	L	H	H	H
24	41 912 Hz	121	L	H	H	H	H	H	H	H	H	H	L
25	42 258 Hz	122	H	L	H	H	H	H	H	L	H	H	H
26	42 604 Hz	123	H	L	H	H	H	H	H	H	H	H	L
27	42 951 Hz	124	H	H	L	H	H	H	H	L	H	H	H
28	43 297 Hz	125	H	H	L	H	H	H	H	H	H	H	L
29	43 643 Hz	126	H	H	H	L	H	H	H	L	H	H	H
30	43 990 Hz	127	H	H	H	L	H	H	H	H	H	H	L

Design and Operation Mode

The table shows the 30 ultrasonic transmission frequencies used in the wireless transmission of remote control commands to the TV receiver. These frequencies are derived from the frequency of an SC-crystal controlled oscillator with the aid of a variable frequency divider operating on the blanking principle. This is accomplished in that 1 ... 30 pulses of every 128 out of 2.2168 MHz pulses are blanked out. The variable divider is preceded by a flip-flop which halves the SC frequency. The variable divider is followed by a fixed divider which divides by 50. It reduces the jitter, which is unavoidable when using the blanking principle, to negligible values. The expression for the ultrasonic output frequency is

$$f_u = \frac{x \cdot f_t}{12\,800}$$

wherein x = 98 to 127, i. e. (128 – 30) to (128 – 1) and f_t = 4.4336 MHz (sub-carrier frequency). The space between two adjacent ultrasonic frequencies is 346.4 Hz.

Upon actuation of one of the double touch contacts 1 to 30 one of the control inputs a ... e and f ... l are simultaneously addressed. In the decoder these input signals are converted into 5-bit words and applied to the variable divider which will then generate the desired ultrasonic frequency.

The command error protection defines any actuation whereby one of the control inputs a ... e and f ... l are addressed inaccurately as a command error. Under these conditions the oscillator will not start to operate, and the frequency divider is held in a defined position. The same applies when none of the touch contacts is touched. Consumption under these standby conditions is very low, so that ultrasonic transmitter need never be switched off. The selected frequency appears at the ultrasonic output when the threshold voltage is exceeded at the two control inputs. A threshold voltage hysteresis ensures that AC voltages which may be superimposed on the input voltage cannot falsify the actuation. The *RC* networks *R3*, *C3* (Fig. 1) protect the inputs from interference and from damage through electrostatic discharges. These *RC* networks may be omitted if mechanical actuated contacts are used. In this case the value of resistor *R2* should be 47 kΩ.

Thirty Channel Ultrasonic Receiver for Remote-Controlled TV Receivers

Monolithic integrated MOS-circuit in silicon-gate technique. The SAA 1025 is intended for remote control systems in which 30 different ultrasonic frequencies are used to transmit 30 control commands. The recommended transmitter is the SAA 1024 produced by INTERMETALL.

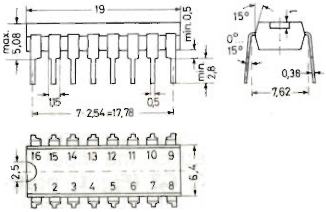
The SAA 1025 measures the frequency of the arriving signal by counting the cycles during a fixed measuring time determined by crystal. Evaluation happens only if two succeeding test cycles give the same result. All ultrasonic commands are converted into a coded 5-bit output signal and issued in pulsed form. Nine of the thirty commands are used internally of the SAA 1025 and serve e. g. for controlling the D/A-converter. The further 21 commands are for free application. Sixteen different TV channels are selectable if a 1 out of 16-decoder is connected to the outputs. For storage the channel information, e. g. the integrated circuits SAS 560 S or SAS 570 S may be used.

Signals for controlling three analogue values, e. g. volume, brightness and colour saturation, are stored in the SAA 1025 and continuously delivered in the shape of square wave voltages. The pulse duty factor of these square wave voltages determines the level of the analog value.

Every control command can also be given directly into the IC.

Fig. 1:
SAA 1025 in dual in-line plastic SOT-38 package
20 A 16 according to DIN 41 866

Weight approximately 1.2 g
Dimensions in mm



Pin connections

1	Ground, 0, V_{SS}	9	In/output C-bit
2	Volume output V	10	Option
3	Brigthness output B	11	In/output B-bit
4	Colour saturation output C	12	In/output A-bit
5	V_{SS}	13	Leave vacant! Test pin
6	Mains switch output	14	Ultrasonic input
7	In/output E-bit	15	Clock input Q
8	In/output D-bit	16	Supply voltage V_{DD}

All voltages are referred to pin 1.

Maximum Ratings

Drain voltage	$-V_{DD}$	20	V
Clock voltage, peak-to-peak	$-V_t$	15	V
Voltage at the other pins	V_n	$-30 \ldots +0.3$	V
Drain currents, pins 2 . . . 4, and 6	$-I_D$	5	mA
Ambient operating temp. range	T_{amb}	$-20 \ldots +65$	°C
Storage temperature range	T_S	$-55 \ldots +125$	°C

Recommended Operating Conditions

Drain voltage	$-V_{DD}$	18 (16.5 . . . 19.5)	V
Ultrasonic input voltage, peak-to-peak	$-V_{14}$	0.5 V . . . V_{DD}	
Input voltage for direct commands	$-V_{IH}$	< 0.8	V
Inputs A . . . E	$-V_{IL}$	> 4	V
Clock voltage, sinusoidal, peak-to-peak	V_t	4 . . . 8	V
Clock frequency (sub-carrier)	f_t	4.4336	MHz

Characteristics at $-V_{DD} = 18$ V, $T_{amb} = 25$ °C

Output resistance with current flowing, pins 2 . . . 4 and 6	r_{on}	< 1	kΩ
Pulse duty factor of the output signal, pins 2 . . . 4	t_p/t_0	1/30 . . . 30/1	
Output frequency, pins 2 . . . 4	f_{out}	8.99	kHz
Switching time per step	t_f	184.8	ms
ON and OFF delay in mains and sound controlling	t_{mains}	669.8	ms
Ultrasonic input frequencies at $f_t = 4.4336$ MHz	see table overleaf		

Table 1: Ultrasonic Input Frequencies at f_f = 4.4336 MHz

n	Frequency	Command	Code E	A	B	C	D
1	33 944,89 Hz	Mains On/Off	H	L	H	H	H
2	34 291,21 Hz	Sound Off	L	L	H	H	H
3	34 637,65 Hz	Colour+	H	H	L	H	H
4	34 984,02 Hz	Normalisation [1])	L	H	L	H	H
5	35 330,40 Hz	Colour –	H	L	L	H	H
6	35 676,78 Hz	Z1	L	L	L	H	H
7	36 023,15 Hz	Brightness+	H	H	H	L	H
8	36 369,53 Hz	Z2	L	H	H	L	H
9	36 715,91 Hz	Brightness –	H	L	H	L	H
10	37 062,28 Hz	Z3	L	L	H	L	H
11	37 408,66 Hz	Volume+	H	H	L	L	H
12	37 755,03 Hz	Z4	L	H	L	L	H
13	38 101,41 Hz	Volume –	H	L	L	L	H
14	38 447,79 Hz	Z5	L	L	L	L	H
15	38 794,16 Hz	Channel 1	H	H	H	H	L
16	39 140,54 Hz	Channel 2	L	H	H	H	L
17	39 486,92 Hz	Channel 3	H	L	H	H	L
18	39 833,29 Hz	Channel 4	L	L	H	H	L
19	40 179,67 Hz	Channel 5	H	H	L	H	L
20	40 526,05 Hz	Channel 6	L	H	L	H	L
21	40 872,42 Hz	Channel 7	H	L	L	H	L
22	41 218,80 Hz	Channel 8	L	L	L	H	L
23	41 565,18 Hz	Channel 9	H	H	H	L	L
24	41 911,55 Hz	Channel 10	L	H	H	L	L
25	42 257,93 Hz	Channel 11	H	L	H	L	L
26	42 604,31 Hz	Channel 12	L	L	H	L	L
27	42 950,68 Hz	Channel 13	H	H	L	L	L
28	43 297,06 Hz	Channel 14	L	H	L	L	L
29	43 643,43 Hz	Channel 15	H	L	L	L	L
30	43 989,81 Hz	Channel 16	L	L	L	L	L

Band width ± 160 Hz

The expression for the ultrasonic input frequency f_u is

$$f_u = \frac{f_f\,(97 + n)}{12\,800}$$

[1]) The command "Normalisation" sets the colour saturation output to a pulse duty factor of 16/15 and the brightness output to a pulse duty factor of 18/13.

Design and Operation Mode

The function of the SAA 1025 will be explained with reference to the various pins.

Pin 1 – ground, 0 V_{SS}
The substrate of the integrated circuit is connected through this terminal with the common positive potential of all supply voltages.

Pin 16, supply voltage, V_{DD}
The supply voltage should be within – 16.5 and – 19.5 V (nominal value: – 18 V). Current consumption is approximately 25 mA.

Pin 5
This pin must be connected to pin 1.

Pin 15 – clock input Q
Pin 15 should be connected via a capacitor to the output of a quartz controlled oscillator containing a colour sub-carrier crystal. The peak-to-peak value of the oscillator output amplitude should be 4 . . . 8 V. In the integrated circuit, the quartz frequency is divided by 16. The whole IC operates in synchronism at the clock frequency of approximately 277 kHz thus produced. The accuracy of this frequency determines the accuracy with which the received ultrasonic signals are processed.

Pin 14 – ultrasonic input
The ultrasonic signals are applied to the ultrasonic input via a capacitor. After the arrival of the first ultrasonic pulse, a set-up time of about 23 ms elapses. Then follows a period of measurement with two times 23.1 ms. Then, after an interval of two times 23.1 ms an output pulse of 23.1 ms duration is produced. For a continuous signal, output pulses succeed one another with time intervals of 184.8 ms. During the entire reception period, a resettable counter monitors the cycle time. If there are spaces between two ultrasonic pulses which are either shorter than 18 µs or longer than 36 µs the signal is not evaluated and the signal-processing circuit is reset. After another 15 µs the receiver is ready to operate again. In this way, spurious frequencies above 55.4 kHz and below 27.7 kHz are rendered ineffective.
The table shows how the 30 receivable ultrasonic frequencies are allocated to the various commands. Signals which are either short of 4 pulses or have a surplus of 4 pulses during the measuring time, owing to frequency variations of the transmitter, are still accepted as correct signals. This means that the ultrasonic transmission frequency of 33.9 kHz may fluctuate by ± 0.51 %, and the frequency of 44.0 kHz by ± 0.39 % without causing errors.

Pins 2, 3 and 4 – D/A outputs C, B and V
The outputs C (colour saturation), B (brightness) and V (volume) are the drain pins of the D/A converter output transistors. A square wave output voltage is produced when resistors are inserted between the outputs and V_{DD}. The frequency of these square wave voltages is approximately 8.9 kHz. The pulse duty factor is variable in 30 steps between 1/30 and 30/1. Approximately 115 ms after the onset of an ultrasonic command, the pulse duty factor is advanced by one step. In the case of a continuous signal, further advances follow at intervals of 184.8 ms until the final value is reached. The time needed to traverse the entire range of variation is 5.544 seconds. For the duration of the pulse, an open-drain output transistor is turned on. Its maximum resistance is 1 kΩ.

When the supply voltage V_{DD} is switched on the D/A outputs are normalised with the following pulse duty factors: output colour saturation = 16/15; output brightness = 18/13; output volume = 10/21. The command n = 4 (see table) sets output C and B also to a pulse duty factor of 16/15 and 18/13, but this command has no effect to the output V. The command n = 2 switches on or off the open-drain transistor at the output V with a delay time of approximately 0.7 s thus acting as a sound On/Off-switch. The sound suppression is also lifted when the TV receiver is switched on after having been switched off.

Pin 10 – option
This terminal allows the operational mode of mains control to be selected. If it is connected to V_{SS}, it will only be possible to block the open-drain transistor at pin 6 (mains off) with the "mains" command. Switching on the mains may be effected by each of the program commands. If pin 10 remains open, then the mains can only be switched on and off by the "mains" command.

Pin 6 – mains switch output
For the purpose of switching the television receiver on or off ultrasonically, the input signal must be available for a least 0.7 seconds. Thereafter, the mains flip-flop is triggered. It controls an open-drain transistor. During the normalisation after V_{DD} is switched on, the mains flip-flop is set in such a way that the output transistor is turned off. The resistance of this transistor is below 1 kΩ when it is turned on. Through pin 6, the mains flip-flop can also be set externally without delay. In that case, pin 6 must be connected to V_{SS} for at least 10 µs. After switch-off, the mains flip-flop remains locked for 23.1 ms, so that renewed switch-on by the connection of pin 6 to V_{SS} can only take place after the lapse of this time. When the output transistor is turned off, the D/A-converters are locked, i. e. the output signals at pins 2, 3 and 4 cannot be varied.

Pins 7, 8, 9, 11 and 12 – control terminals
Pins 7 . . . 12 serve as inputs for commands originating at the television receiver itself and, at the same time, as outputs for ultrasonically transmitted commands. Since the inputs of the MOS circuit have a very high impedance, actuation by means of touch contacts is possible. The leakage currents of the integrated protection diodes connected to the inputs amount to less than 100 nA at room temperature.
A coded command given with the aid of touch contacts is transferred in the same manner via open-source transistors. Characteristics of these output transistors are shown in Fig. 4. Under this condition the SAA 1025 operates as impedance converter.
Fig. 2 shows a recommended circuit for driving pins 7 . . . 12 via touch contacts, whilst Fig. 3 illustrates the connection of TTL-ICs to these pins. All the 30 feasible commands must be coded according to the table 1 for addressing the five inputs A . . . E. Since the leakage currents of the input diodes contained in the TTL circuits (emitter diodes of the multi-emitter transistor) are too high, pins 7 . . . 12 of the MOS circuit should be isolated from the TTL inputs by diodes.
While the touch contact is inoperative, the MOS input is pulled towards zero potential by means of the resistor *R1*. The existing leakage currents must not produce a voltage drop across *R1* of more than 0.8 V if a signal-to-noise ratio of 0.8 V is to be maintained with respect to the minimum threshold of 1.6 V. When the touch contact is actuated, current flows through the resistors *R1*, *R2* and *R3*. If the voltage at the input exceeds the threshold, the input transistor starts to conduct and a corresponding signal is transmitted. As the maximum threshold may amount to 2.6 V, suitable dimensioning of the resistors *R1*, *R2* and *R3* will ensure that

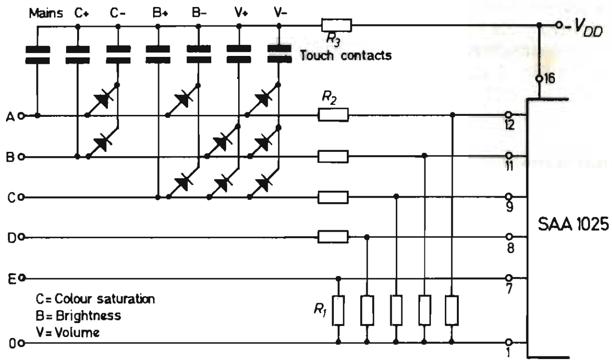


Fig. 2: Arrangement of the touch contacts

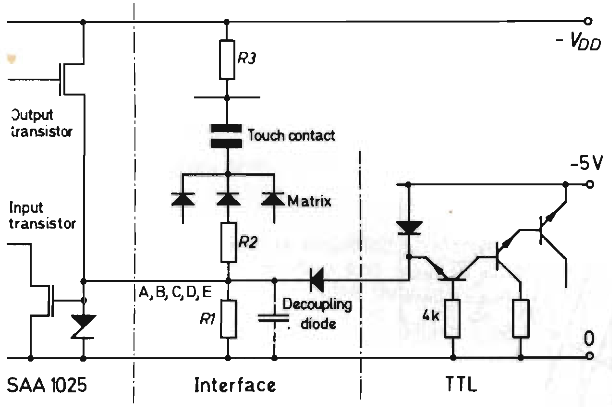


Fig. 3: External circuitry for pins 7 . . . 12

an adequate input signal is always available, having due regard to the signal-to-noise ratio.

As the voltage rises, the decoupling diode starts to conduct when a level of approximately – 4.5 V has been reached, and this prevents the voltage from rising further. The resistors *R2* and *R3* should be large enough to prevent the current from the TTL input from rising sufficiently high for the TTL circuit to be activated even in the case of a possible short-circuit at the touch contact. This condition can easly be fulfilled in view of the high rating of the protective resistors in series with the touch contact, prescribed for safety reasons.

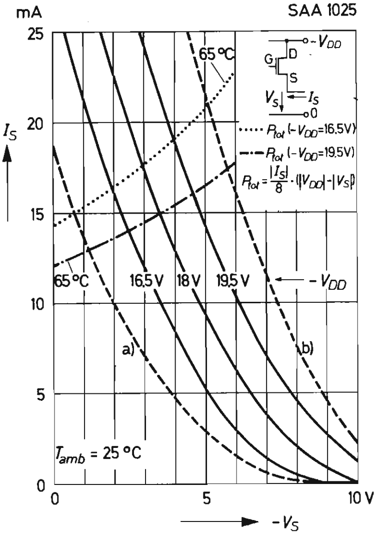
If necessary, the inputs should be provided with protective capacitors, to provide additional protection against stray fields. If the input threshold voltage is nevertheless exceeded due to isolated surges, for example picture tube flash-overs, such interference is rendered ineffective by an integrated protective logic. An input signal is only recognized as valid if it exceeds the threshold voltage at least once in each of three suc-

cessive 23.1 ms periods for at least 10 µs. When this happens, an output pulse of approximately 23.1 ms duration is transmitted after a processing period lasting approximately 46.2 ms. During the output pulse, the output transistor shown in Fig. 3 conducts current, i. e. its resistance falls below 1 kΩ. As a result, the TTL circuit shown in Fig. 3 may be activated, for example.

The output signal transmitted from pins 7 . . . 12 acts again upon the input, but this cannot cause interference because the inputs are locked while an output signal is transmitted. If commands are issued both ultrasonically and via the contacts at the television receiver, the direct command will always override the ultrasonic command. The coded signals listed in the table are always transmitted in pulse form by the SAA 1025 no matter whether the command has been issued either ultrasonically or by a contact at the television receiver. This provides the further facility of controlling additional indicating devices.

Fig. 4:
Characteristics of the open-source output transistors at pins 7 . . . 12, with admissible power dissipation hyperbolae [1])

a) - - - - Limit of spread for $-V_{DD} = 16.5$ V
b) - - - - Limit of spread for $-V_{DD} = 19.5$ V



[1]) These hyperbolae refer to a single transistor. All five output transistors may operate simultaneously with the indicated power dissipation.

Block Diagram of the SAA 1025

The block diagram of Fig. 5 shows the internal organisation of the SAA 1025.

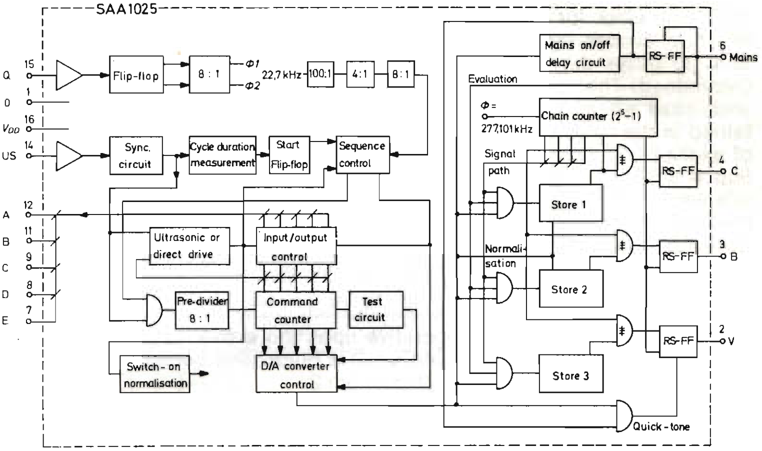


Fig. 5: Block diagram of the SAA 1025

The 4.4 MHz input signal is amplified and drives a clock generator consisting essentially of a flip-flop and an 8 by 1 divider and produces a 2-phase clock signal with a pulse duty factor of 3/8 to 5/8 at 277 kHz. Connected to the clock generator is a 3200 by 1 divider which delivers pulses with a 23.1 ms spacing for control purposes and for determining the measuring time.

The ultrasonic signal is amplified in a preamplifier and then synchronised with the operational clock signal. The signals thus obtained are fed to the circuit which measures the duration of the cycle. If this measurement reveals too long or too short a cycle, the sequence control is reset, and the measuring cycle restarted.

On a second path, an 8 by 1 pre-divider is controlled by the synchronised ultrasonic signals. This divider determines the channel spacing. The command counter is connected to this pre-divider. Together with the test circuit, this command counter forms a 7-bit binary counter. The test circuit ensures that the 5-bit command counter performs three complete counts before the result is evaluated. This excludes the possibility that frequencies which are a multiple or a fraction of useful frequencies produce wrong commands. The command counter comprises a 5-bit register whose contents are compared with the result of the repeat measurement before a command can be evaluated.

All commands are delivered in coded form via the input/output control system to outputs A to E in the form of pulses. The input/output control system ensures also that the command counter is set when commands are produced directly at the input of the TV-receiver.

A switch-on normalisation arrangement ensures that all counters and storage devices are set to the desired initial positions when the supply voltage is switched on. This will only happen when both clock pulses operate correctly. The D/A converter control system recodes the commands, so that the latter can be used to set the storage devices of the D/A converters accordingly.

The basic clock for the D/A output signals is generated by a chain counter which divides the operational frequency by 31. In this way, the available 30 pulse duty factors of the D/A squarewave output signals are determined. The three storage devices consist of five flip-flop stages in each case which can be set in the parallel mode. The information contained in the chain counter is compared with the stored signals by means of exclusive OR elements. In the case of coincidence, the RS output flip-flop is set, and reset every time zero is passed in the chain counter. In this way, three squarewave output signals are obtained having the same frequency determined by the chain counter, their pulse duty factors being fixed by the information contained in the storage device. The latter is changed by parallel conversion in conjunction with information from the chain counter.

An on/off delay is rendered operative upon the arrival of switching commands for the mains flip-flop and when a quick-tone command is issued. The latter blocks the output flip-flop at pin 2.

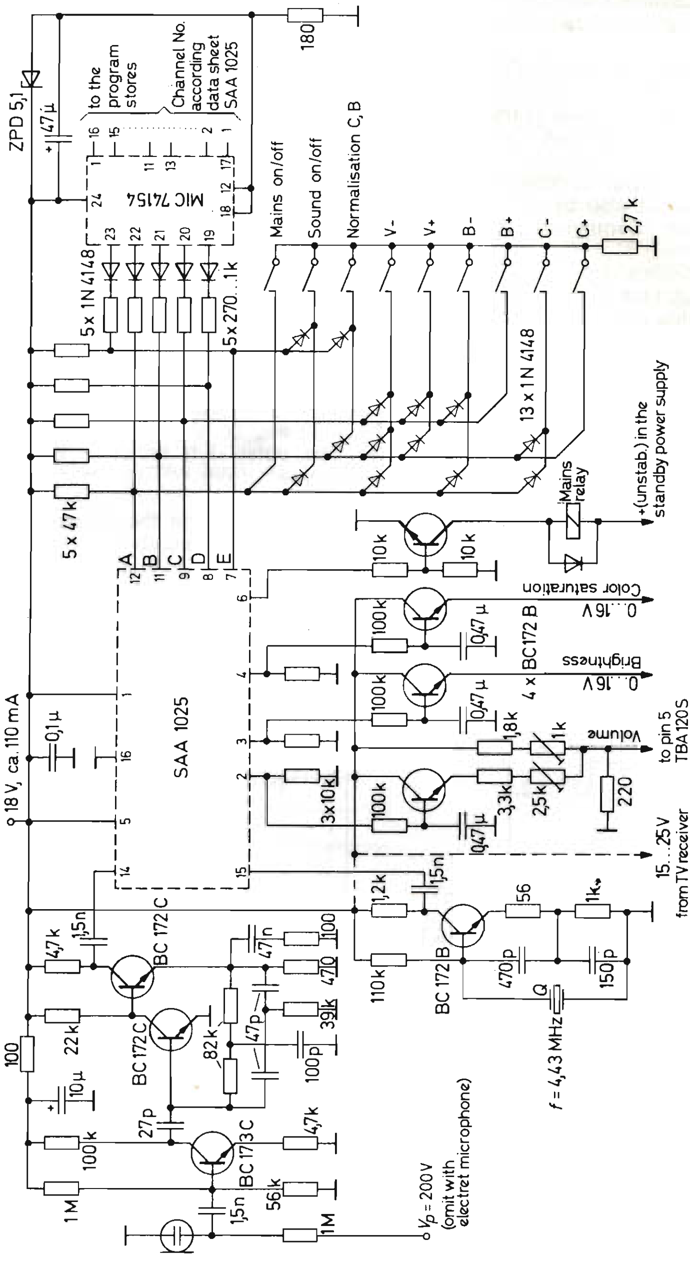


Fig. 6: Complete TV remote control circuit arrangement using the SAA 1025

Thirty Channel Ultrasonic Receiver with Program Store
for television and radio receivers, remote-controlled without cable.

Monolithic integrated MOS-circuit in silicon-gate technique. The SAA 1130 is intended for remote control systems in which 30 different ultrasonic frequencies are used to transmit 30 control commands. The recommended transmitter is the SAA 1024 produced by INTERMETALL.

The 30 control commands can be given not only by ultrasonic transmission, but also by direct inputs to the IC. Furthermore, the additional command "Sequential program change" can be fed to the IC via direct inputs.

The SAA 1130 measures the frequency of the arriving signal by counting the cycles during a fixed measuring time determined by crystal. All ultrasonic commands are converted into a coded 5-bit output signal. The outputs of the SAA 1130 are TTL-compatible.

Signals for controlling three analog values, e. g. volume, brightness and color saturation, are stored in the SAA 1130 and continuously delivered in the shape of square wave voltages. The pulse duty factor of these signals determines the level of the analog value.

The program outputs PA ... PD are provided for driving the IC combination SAA 1020/SAA 1021 by INTERMETALL. This combined device digitally generates and stores the tuning voltages for the variable capacitance diodes of the tuner and the band-switching signals. Moreover, these outputs serve for driving the character generator SAA 1008 which performs the visual display of the program number on the television screen. In the block diagram of Fig. 1, these two possibilities have been indicated.

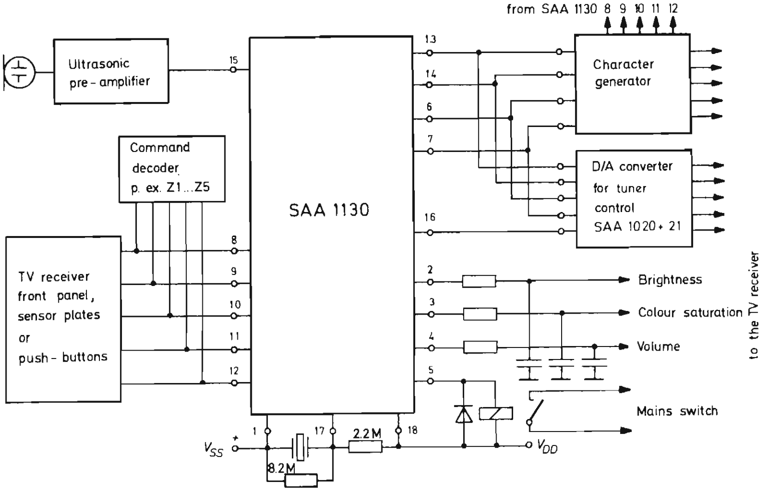
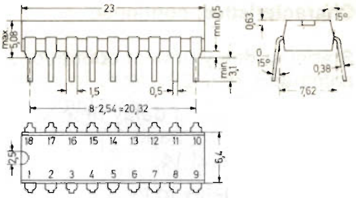


Fig. 1: Block diagram of an ultrasonic remote-control system equipped with the SAA 1130, including generation of the tuning voltage with the SAA 1020/SAA 1021, and program number display by means of SAA 1008

Fig. 2:
SAA 1130 in plastic package
20 A 18 according to DIN 41 866

Weight approximately 1.3 g
Dimensions in mm



Pin connections

1	Ground, 0, V_{SS}	10	B-bit control terminal
2	Brightness output B	11	A-bit control terminal
3	Color saturation output C	12	E-bit control terminal
4	Volume output V	13	Program output PA
5	Mains switch output M	14	Program output PB
6	Program output PC	15	Ultrasonic input U
7	Program output PD	16	Input/output T
8	D-bit control terminal	17	Quartz terminal Q
9	C-bit control terminal	18	Supply voltage V_{DD}

All voltages are referred to pin 1 *(V_{SS}).*

Maximum Ratings

Drain voltage	$-V_{DD}$	20	V
Voltage at the other pins	V_n	$-30 \ldots +0.3$	V
Output currents	$-I_D$	5	mA
Ambient operating temperature range	T_{amb}	$-20 \ldots +65$	°C
Storage temperature range	T_S	$-55 \ldots +125$	°C

Recommended Operating Conditions

Supply voltage	$-V_{DD}$	18 (16.5 . . . 19.5)	V
Ultrasonic input voltage, peak-to-peak, coupled capacitively	V_{US}	0.5 V. . .V_{DD}	
Input voltages for direct commands, pins 8 . . . 12	$-V_{IH}$ $-V_{IL}$	≤ 0.8 ≥ 4	V V
Clock frequency (sub-carrier freq.)	f_t	4.4336	MHz

Characteristics at $-V_{DD} = 18$ V, $f_t = 4.4336$ MHz, $T_{amb} = 25$ °C

Current consumption	$-I_{DD}$	25	mA
Voltage drop across the open-drain output transistors at $-I_O = 1$ mA, pins 2 . . . 7, 13 and 14	ΔV	< 0.6	V
Output frequency, pins 2 . . . 4	f_o	17.6	kHz
Pulse duty factor of output signal, pins 2 . . . 4	t_p/t_0	1/62 . . . 62/1	

Characteristics, continued

Stepping delay time at continuous command, pins 2 . . . 4	t_f	138.6	ms
Program stepping delay time at continuous command, pins 6, 7, 13 and 14	t_f	692.9	ms
On and Off delay in mains controlling	t_M	692.9	ms

Table 1: Ultrasonic input frequencies at f_t = 4.4336 MHz and output code

Ultrasonic channel No	Center frequency Hz	Command	Output code pins 8 . . . 12 E	A	B	C	D
–	–	Sequential progr. change	L	H	H	H	H
1	33 944.89	Mains Off	H	L	H	H	H
2	34 291.21	Sound Off	L	L	H	H	H
3	34 637.65	Color saturation +	H	H	L	H	H
4	34 984.02	Normalisation	L	H	L	H	H
5	35 330.40	Color saturation –	H	L	L	H	H
6	35 676.78	Additional command Z1	L	L	L	H	H
7	36 023.15	Brightness +	H	H	H	L	H
8	36 369.53	Additional command Z2	L	H	H	L	H
9	36 715.91	Brightness –	H	L	H	L	H
10	37 062.28	Additional command Z3	L	L	H	L	H
11	37 408.66	Volume +	H	H	L	L	H
12	37 755.03	Additional command Z4	L	H	L	L	H
13	38 101.41	Volume –	H	L	L	L	H
14	38 447.49	Additional command Z5	L	L	L	L	H
15	38 794.16	Program 1	H	H	H	H	L
16	39 140.54	Program 2	L	H	H	H	L
17	39 486.92	Program 3	H	L	H	H	L
18	39 833.29	Program 4	L	L	H	H	L
19	40 179.67	Program 5	H	H	L	H	L
20	40 526.05	Program 6	L	H	L	H	L
21	40 872.42	Program 7	H	L	L	H	L
22	41 218.80	Program 8	L	L	L	H	L
23	41 565.18	Program 9	H	H	H	L	L
24	41 911.55	Program 10	L	H	H	L	L
25	42 257.93	Program 11	H	L	H	L	L
26	42 604.31	Program 12	L	L	H	L	L
27	42 950.68	Program 13	H	H	L	L	L
28	43 297.06	Program 14	L	H	L	L	L
29	43 643.43	Program 15	H	L	L	L	L
30	43 989.81	Program 16	L	L	L	L	L

Explanation of the Commands

The additional command Z1 is provided for the recall of the program number display on the TV screen by means of the INTERMETALL character generator SAA 1008. The additional commands Z4 and Z5 act upon pin 16 (T) through which, via the D/A-converter SAA 1020/1021 for tuner control, fine tuning of the tuner is carried out. The additional commands Z2 and Z3 are available for further applications which may be required.

The TV receiver is switched on – with a delay of approximately 0.7 seconds – if either one of the program selection commands 1 . . . 16 or the sequential program change command is given. The sound Off command results in the open-drain transistor at the volume output being blocked, again with a 0.7 second delay. Sound is restored without delay if one of the commands "sound Off", "volume +" or "volume –" is given.

The command "normalisation" has the effect of causing the output signals at the color saturation and brightness outputs to assume the pulse duty factor 32/31.

The center frequencies of the ultrasonic channels indicated by the table 1 are determined in accordance with the clock frequency by the equation given below:

$$f_{us} = \frac{f_t \cdot (97 + \text{US channel No})}{12\,800}$$

Design and Operation Mode of the SAA 1130

The function of the SAA 1130 will be explained with reference to the various pins.

Pin 1 – ground, 0, V_{SS}
Positive pole of the supply voltage. All voltages are referred to this potential.

Pin 18 – supply voltage V_{DD}
Negative pole of the supply voltage

Pins 2, 3 and 4 – analog outputs brightness, color saturation and volume
These three outputs are the drain terminals of the D/A-converter output transistors. A square wave output voltage is produced when resistors are inserted between the outputs and V_{DD}. The frequency of these square wave voltages is approximately 17.5 kHz, the pulse duty factor being variable in 62 steps between 1/62 and 62/1. The given information is contained in the pulse duty factor and thus in the mean value of the potential drop which occurs across the external load resistor. After smoothing by *RC* networks, direct voltages are obtained whose amplitude determines brightness, volume and color saturation respectively.

Approximately 115 ms after the onset of an ultrasonic command, the pulse duty factor is advanced by one step. In the case of a continuous signal, further steps follow at intervals of 138.5 ms until the final value is reached. The time needed to traverse the entire range of variation is 8.5 seconds. For the duration of the pulse, the open-drain output transistor is turned on, having a voltage drop of max. 0.6 V at 1 mA output current.

When the supply voltage is switched on the output signals of the analog outputs are normalised to the pulse duty factor 32/31. About 0.7 seconds after the onset of the sound Off command, the open-drain transistor at pin 4 is blocked. The sound is restored without delay when one of the commands "sound Off", "volume +" or "volume −" is given. The sound suppression is also lifted when the TV receiver is switched on after having been switched off.

Pin 5 — mains switch output M
Connected to this output is the drain terminal of an open-drain transistor which, in the On-condition of the TV receiver, effects a voltage drop of less than 0.6 V at 1 mA output current. With an admissible output current of −5 mA and a supply voltage of 18 V, a relay can be driven directly from pin 5 if its coil resistance is at least 3 kΩ. However, activation of a driver transistor, a thyristor or a triac is equally feasible. The output transistor is controlled by the mains flip-flop.

If the TV receiver is to be switched on or off either ultrasonically or by direct command, this command will have to be maintained for at least 0.7 seconds before the mains flip-flop responds. If, after the supply voltage V_{DD} has been applied, the SAA 1130 is normalised by its internal On-standardisation, the mains flip-flop will assume a position which results in a blocked output transistor. At the same time, the blocked output transistor causes the D/A-converters to lock, so that the pulse duty factors of the output signals appearing at the analog outputs cannot change while the TV receiver is switched off.

There are three ways in which the TV receiver can be switched on:

by any of the 16 program commands;

by the command "sequential program change" which can only be effected by direct input; or

by connecting pin 5 to V_{SS} for at least 10 µs.

The TV receiver is switched off by a "mains Off" command. After switch-off, the mains flip-flop remains locked for 23.1 ms, so that renewed switch-on by the connection of pin 5 to V_{SS} can only take place after the lapse of this time.

Pins 8 . . . 12 — A-bit . . . E-bit control terminals

Pins 8 . . . 12 serve as inputs for commands originating at the TV receiver itself and, at the same time, as outputs for ultrasonically transmitted commands. Since the inputs of the MOS circuit have a very high impedance, actuation by means of touch contacts is possible. The leakage currents of the integrated protection diodes connected to the inputs amount to less than 100 nA at 25 °C. Fig. 3 shows a circuit arrangement suggested for driving the pins 8 . . . 12 by means of touch plates. Fig. 4, moreover, illustrates how a TTL circuit may be driven by pins 8 . . . 12.

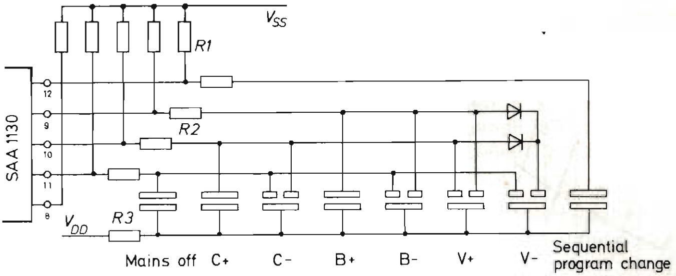


Fig. 3: Driving the control terminals pins 8 . . . 12 by touch plates on the TV set

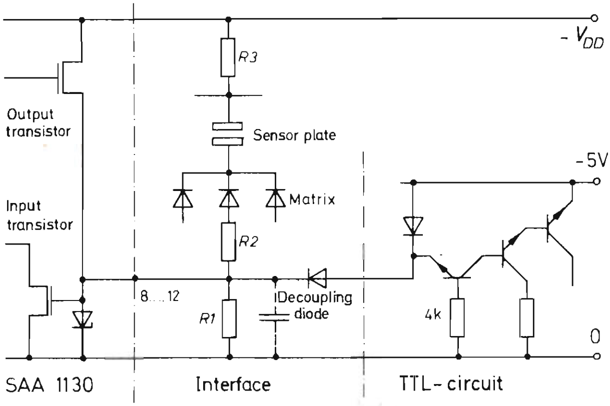


Fig. 4: Diagram showing how the SAA 1130 is connected to a TTL circuit

If all or some of the 31 envisaged commands are to be fed directly to the IC, they will have to be coded according to the table 1 shown on page 54. If such a coded command is issued by an electronic touch plate, it will be issued in the same code as a low-ohmic pulse via the open-source output transistor at pins 8 . . . 12. In this mode the SAA 1130 acts as an impedance transformer. The characteristics of the output transistors are illustrated in Fig. 5.

Since the leakage currents of the input diodes contained in the TTL circuits (emitter diodes of the multi-emitter transistor) are too high, pins 8 . . . 12 of the MOS circuit should be isolated from the TTL inputs by diodes (Fig. 4). While the touch contact is inoperative, the MOS input is pulled towards zero potential (V_{SS}) by means of the resistor *R1*. These leakage currents must not produce a voltage drop across *R1* of more than 0.8 V if a signal-to-noise ratio of 0.8 V is to be maintained with respect to the minimum threshold of 1.6 V.

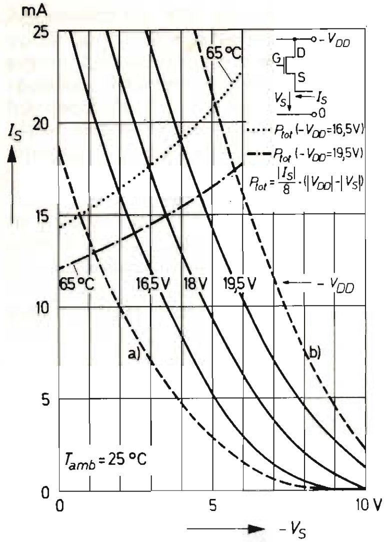


Fig. 5: Characteristics of the open-source output transistors at pins 8...12, with admissible power dissipation hyperbolae. These hyperbolae refer to a single transistor. All five output transistors may operate simultaneously with the indicated power dissipation.

a) ----- limit of spread for $-V_{DD}$ = 16.5 V

b) ----- limit of spread for $-V_{DD}$ = 19.5 V

When the touch contact shown in Fig. 4 is actuated, current flows through the resistors *R1*, *R2* and *R3*. If the voltage drop across resistor *R1* exceeds the specified V_{IL} minimum value of 4 V, the input transistor conducts, and a corresponding signal is transmitted. Suitable dimensioning of the resistors *R1*, *R2* and *R3* will ensure that an adequate input signal is always available, having due regard to the signal-to-noise ratio. As the input voltage rises, the decoupling diode starts to conduct when a level of approximately − 4.5 V has been reached, and this prevents the input voltage from rising further. The resistors *R2* and *R3* have to be large enough to prevent the current from the TTL input from rising sufficiently high for the TTL circuit to be activated even in the case of a possible short-circuit of the touch plates. This condition can easily be fulfilled in view of the high rating of the protective resistors in series with the touch plates prescribed for safety reasons (see VDE 0860).

If necessary, the inputs should be provided with protective capacitors, to give additional protection against stray fields, see Fig. 4. If the input threshold voltage is nevertheless exceeded due to isolated surges, for example picture tube flash-overs, such interference is rendered ineffective by a built-in protective logik. An input signal is only recognized as valid if it surpasses the threshold voltage within three 23.1 ms cycles for at least 10 µs per cycle. When this happens, an output pulse of 23.1 ms duration is transmitted after a processing period lasting 46.2 ms. During

this output pulse, the output transistor shown in Fig. 4 is conducting. As a result, the TTL circuit shown in Fig. 4 may be activated, for example.

The output signal transmitted from pins 8 . . . 12 acts again upon the inputs, but this cannot cause interference because the inputs are locked while an output signal is transmitted. If commands are issued both ultrasonically and via the contacts at the TV receiver, the direct command will always override the ultrasonic command.

The coded input signals listed in the table 1 are transmitted by the SAA 1130 always in the shape of pulses, irrespective of whether the command is issued ultrasonically or directly. It is therefore possible, for example, to drive additional indicating devices by means of the SAA 1130.

Pins 6, 7, 13 and 14 – program outputs PA . . . PD

From these outputs the information on the selected program can be obtained statically in binary-coded form. The code is shown by the table 2. The output transistors are open-drain transistors whose voltage drop is below 0.6 V at an output current of 1 mA.

TV programs are chosen either selectively (by the commands "Program 1 . . . Program 16") or sequentially (command "Sequential program change"). For sequential program selection, the program information is changed step-wise in the upward sense. If the "Sequential program change" command is given continually, the first change of program takes place after 115 ms, and every further change at 0.7 second intervals. After program 16 has been reached, it is followed again by program 1.

When the supply voltage V_{DD} is applied to the SAA 1130, the program store is automatically set to program 1. If the TV receiver is switched on by the command "Sequential program change", this command is bound to be interrupted after switch-on, before further program-stepping is rendered possible by a new command being issued.

Pin 15 – ultrasonic input U

Ultrasonic signals amplified to at least 500 mV (peak-to-peak) are applied to this input via a capacitor. The integrated input amplifier is biased automatically and has an input resistance exceeding 1 MΩ.

The first ultrasonic pulses arriving at pin 15 are followed by a preparatory period of approximately 23 ms. Then follows a measuring period of twice 23.1 ms. After an interval of twice 23.1 ms, this is followed at the pins 8 . . . 12 by an output pulse of 23.1 ms duration, coded according to the table 1. The execution of those commands being processed in the SAA 1130 itself also takes place during these output pulses. If a permanent signal appears at the ultrasonic input, the interval between the output pulses amounts to 138.5 ms.

During the entire reception period, a resettable counter tests the duration of the input signal periods. If the intervals between any two ultrasonic pulses are less than 20.7 μs or greater than 31.6 μs, the signal is not evaluated, and the evaluation circuit is reset to its initial state. After about 15 μs, the ultrasonic receiver's readiness to receive signals is restored. In this way, undesired signals at frequencies below 31.6 kHz and above 48.3 kHz are rendered ineffective.

Pin 16 – input/output T

Pin 16 is an input as well as an output terminal. When the SAA 1130 is tested it serves as input for a blocking signal. If Z4 or Z5 command is issued, the SAA 1130 transmits, in addition to the binary-coded output signal at pins 8 . . . 12, a further output signal in the shape of a pulse at pin 16 whose duration, in the case of a Z4 command, is 21.6 μs and, in the case of a Z5 command, 23.1 ms. These pulses actuate the fine tuning of the tuner via the tuner control IC set SAA 1020/SAA 1021 by INTERMETALL.

Pin 17 – quartz terminal Q
A color sub-carrier crystal (4.4336 MHz) is connected between this pin and V_{SS}. A 5.6 MΩ resistor between pin 17 and V_{DD} determines the bias of the integrated oscillator circuit. The accuracy of the crystal-controlled frequency determines the evaluation accuracy of the ultrasonic receiver.

Table 2: Output code at pins 6, 7, 13 and 14

Program number	Code PA	PB	PC	PD
1	L	L	L	L
2	H	L	L	L
3	L	H	L	L
4	H	H	L	L
5	L	L	H	L
6	H	L	H	L
7	L	H	H	L
8	H	H	H	L
9	L	L	L	H
10	H	L	L	H
11	L	H	L	H
12	H	H	L	H
13	L	L	H	H
14	H	L	H	H
15	L	H	H	H
16	H	H	H	H

Block Diagram of the SAA 1130

Fig. 6 is a block diagram which shows the internal layout of the SAA 1130. These will now be explained in further detail.

The integrated 4.4 MHz oscillator drives a clock generator which, essentially, consists of two 2 by 1 dividers and an 8 by 1 divider. This generator produces a 1 MHz and a 277 kHz two-phase clock signal. The slow clock has a pulse duty factor of 3/5. Its purpose is to synchronise the whole IC, except the D/A-converter and the cycle counter.

The 6 400-by-1 divider produces the stepping clock signal for the operation control. This unit is the central control unit of the ultrasonic receiver. It determines the measuring times and the entire time sequence of command evaluation.

The ultrasonic signal is fed to a preamplifier via pin 15 and then synchronised with the operational clock signals. The measurement of the cycle time takes place by resetting a counter clocked with a 1.1 MHz frequency. If the counter is reset before a predetermined count has been attained, then the ultrasonic frequency was too high. If the counter reaches its final position, then the ultrasonic frequency was too low. In either case the evaluation of the ultrasonic signal will be interrupted at once, i. e. the operation control unit is reset and the test cycle recommences.

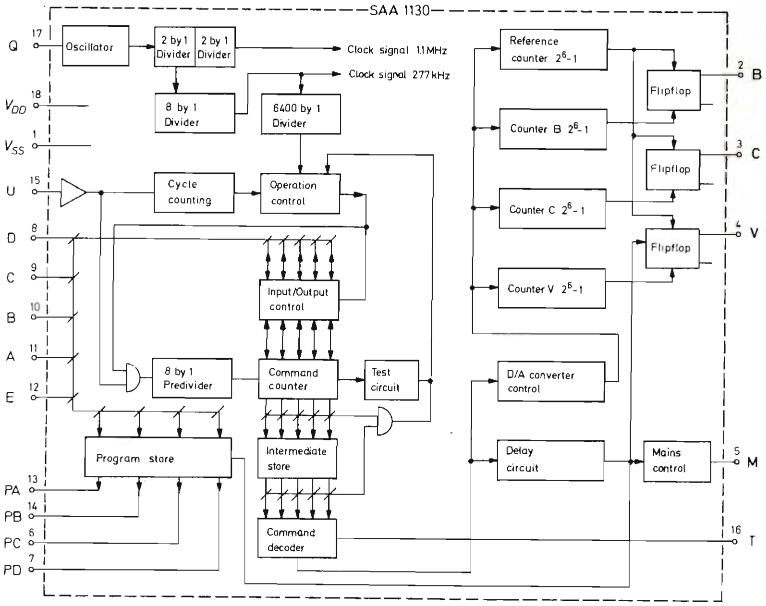


Fig. 6: Block diagram of the SAA 1130

The synchronised ultrasonic signal is also taken to an 8-by-1 divider. The 320 Hz spacing between ultrasonic channels is determined by this divider, to which the 5-bit command counter and a 2-bit test counter are connected. This test circuit ensures that the command counter will have performed three counts before the result is evaluated. The count of the command counter is stored in the intermediate store after the first counting operation. After the second counting operation, the new count of the command counter is compared with the information contained in the intermediate store. Evaluation takes place only if parity has been achieved.

All commands which have been issued are transmitted in pulsed shape to outputs A . . . E (pins 8 . . . 12) via an input/output control unit. In the case of direct feed-in, this control unit ensures that the command counter is set correctly.

The program store is provided in the form of a settable 4-bit binary counter. In the standby condition, program information is stored.

The D/A-converter is a pulse width modulator. It consists of four chain counters, three RS flip-flops and the control unit. The chain counters divide the high clock frequency (1.1 MHz) by 63. In this way, the 62 feasible pulse duty factors of the square wave output signals at the analog outputs (pins 2 . . . 4) are being determined. A chain counter and an RS flip-flop are allocated to the three outputs in each case. In the normalised mode, the zero passage of the reference counter is displaced by 32 counts in comparison with the zero passages of counters B, C or V. If the reference counter reaches zero, all the output flip-flops are set in such a way that the output transistor conducts. On zero passage of the counters B, C or V, the respective flip-flop is reset and the output transistor blocked. At the output, a square wave voltage with a pulse duty factor of 32/31 is thus created. If this factor is to be varied, then the associated counter is held back by one clock cycle while the reference counter and the other two chain counters continue their count. Owing to this retardation, the counter concerned reaches zero passage one clock cycle later, and the pulse duty factor at the output will now be 33/30. A variation of the pulse duty factor in the other sense is obtained in that the relevant chain counter completes its count and the reference counter and the other two chain counters are held back by one clock cycle. In that case the pulse duty factor of the associated analog output will be 31/32.

The delay circuit is activated in the case of the change-over commands for the mains flip-flop and in the case of a quick-tone command.

An internal normalisation arrangement ensures that all counters and storage devices are reset to the desired initial position when the supply voltage V_{DD} is switched on.

Controlled Pulse Generator

Monolithic integrated circuit for pulse separation and line synchronization in television receivers.

The TAA 790, comprising the sync separator with noise suppression, the phase comparator, a switching stage for automatic changeover of noise immunity, and the line oscillator, is designed to replace the shaded part in the block diagram of a conventional television receiver (see Fig. 1). The feedback of the reference pulses from the line transformer to the phase comparator is no longer required, since the control loop for the line synchronization is closed within the TAA 790. Thus synchronization is not dependent on the shape of the flyback pulse.

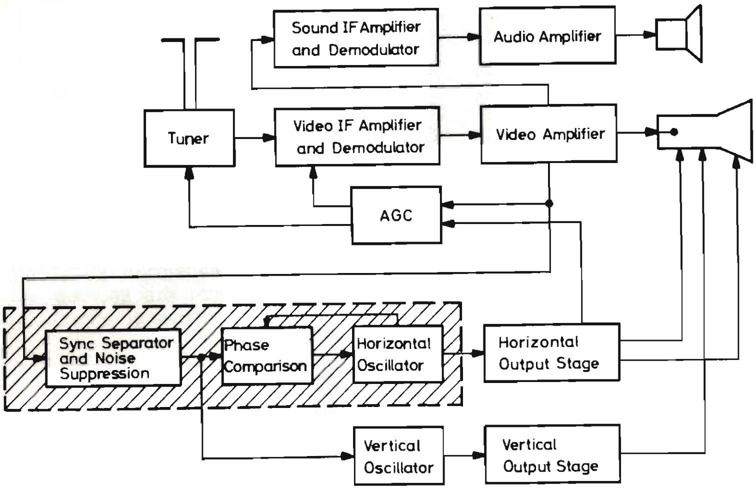
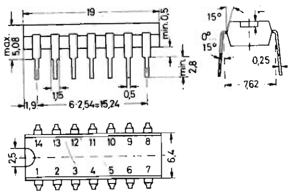


Fig. 1: Block diagram of a conventional television receiver

Fig. 2:
TAA 790 in dual in-line (Dil) plastic TO-116 package
20 A 14 according to DIN 41 866

Weight approx. 1.1 g
Dimensions in mm



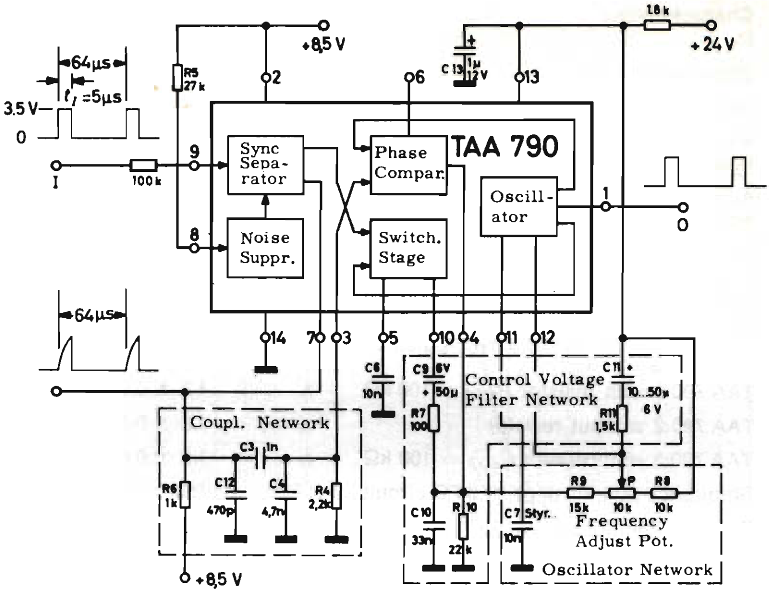


Fig. 3: Test circuit. Tolerance of all external components ± 1 %.

All voltages are referred to pin 14.

Maximum Ratings

Voltages	V_2	10	V
	V_8, V_9	–5	V
	V_6	0 V . . . V_{13}	
	V_7	20	V
Currents	I_7	10	mA
	I_8, I_9	1	mA
Power dissipation at pin 13	$V_{13} \cdot I_{13}$	160	mW
Ambient operating temp. range	T_{amb}	0 . . . +60	°C

Recommended Operating Conditions for the circuit shown in Fig. 3

Voltage at pin 2	V_2	8.5	V
Input video signal (pos. sync pulses)	V_{Ipp}	2 . . . 5	V
Currents	I_8	0.3 (> 0.1)	mA
	I_9	50 (> 20)	µA
	I_{13}	8	mA

Characteristics
for T_{amb} = 25 °C, f_o = 15 625 Hz [1]) in the test circuit Fig. 3

Stabilized voltage	V_{13}	8.5	V
Current consumption	I_2	6 . . . 14	mA
Amplitude of the line and frame sync pulses	V_{7pp}	6.5	V
Amplitude of the output pulses (pin 1 unloaded)	V_{1pp}	2	V
Output resistance at pin 1	$R_{out\,1}$	1	kΩ
Output pulse duration	t_1	11 . . . 16	µs
Phase shift between leading edges of output pulse V_1 and line sync pulse V_7 (see Fig. 4 . . . 7 [2]))			
TAA 790:1 with resistor $R_{6/14}$ = 100 kΩ	t_v	1.2 ± 0.5	µs
TAA 790:2 without resistor	t_v	1.2 ± 0.5	µs
TAA 790:3 with resistor $R_{6/13}$ = 100 kΩ	t_v	1.2 ± 0.5	µs
Frequency pull-in range of AFC circuit	$\pm\Delta f$	750	Hz
Slope of AFC circuit	df_o/dt_v	2	kHz/µs

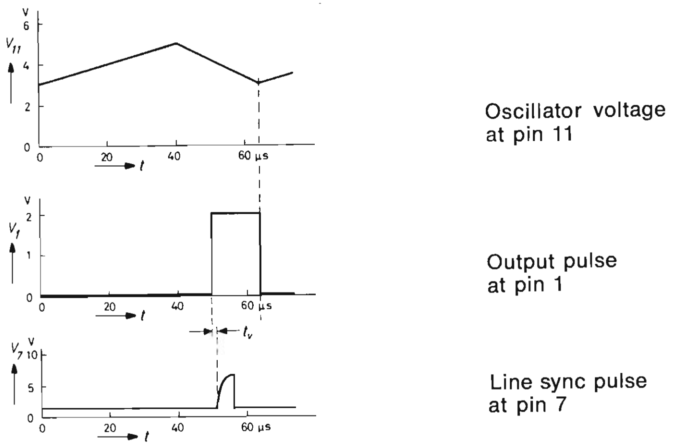


Fig. 4: Oscillator voltage V_{11}, output pulse V_1, and line sync pulse V_7 as a function of time.

[1]) Line frequency to German TV standard. By modifying the value of C7, the TAA 790 can also be used for other TV standards.

[2]) No special delivery of types of a certain group is possible.

Fig. 5:
Positive time shift
(image to the right)
as a function of the resistance
between pins 6 and 13

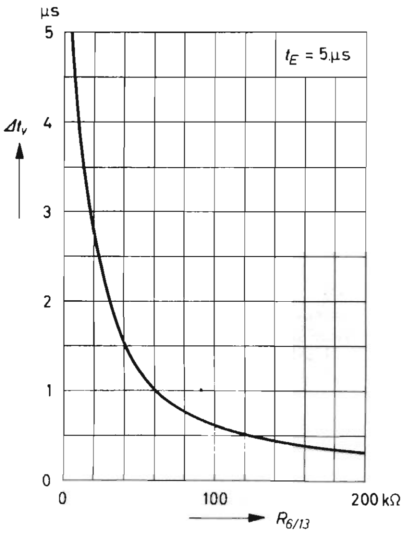


Fig. 6:
Negative time shift
(image to the left)
as a function of the resistance
between pins 6 and 14

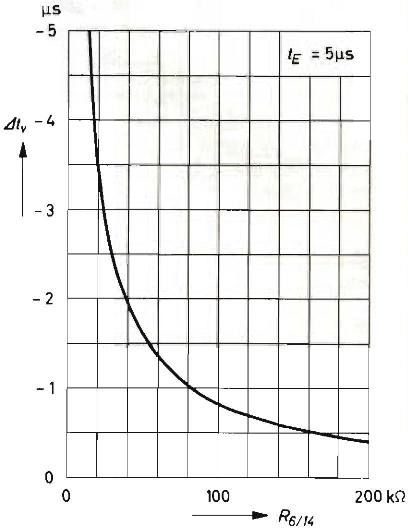
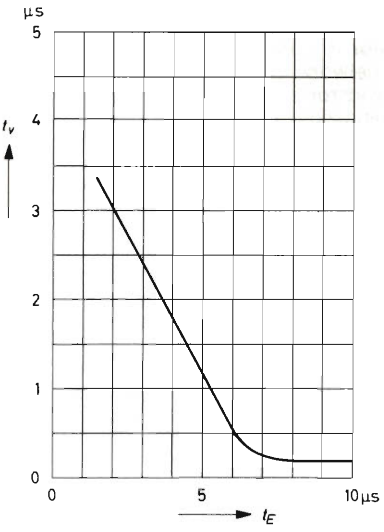


Fig. 7:
Time shift versus duration of
input pulses at pin 9



Design and Operating of the TAA 790

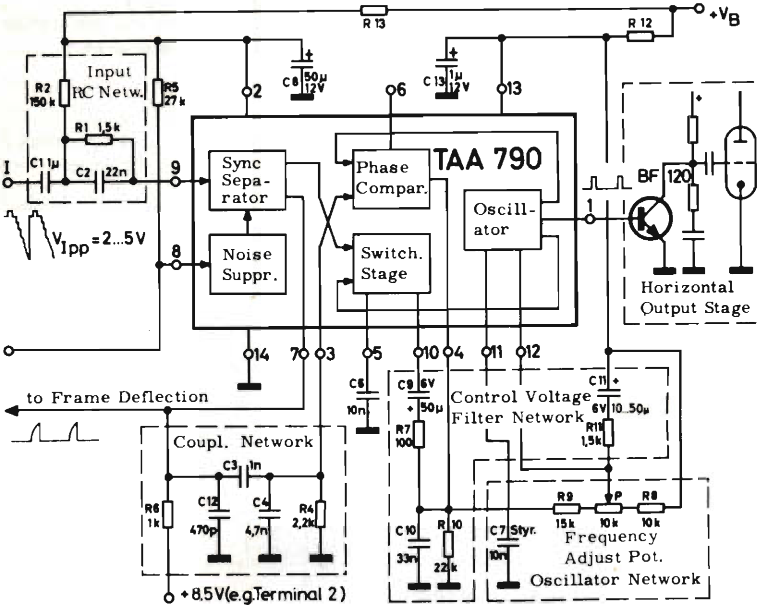


Fig. 8: Operating circuit

The two-stage sync separator separates the synchronizing pulses from the composite video signal. A noise suppression signal may be applied to pin 8. In the phase comparator, the differentiated output pulses of the sync separator are compared with a signal derived from the oscillator. The output signal of the phase comparator is connected to the control input of the oscillator through a filtering network, whose parameters are changed depending on the state of synchronism. A switching stage changes the filtering network to large bandwidth operation in the non-synchronous state, which facilitates pull-in and ensures noise-free operation in the synchronous state. With the addition of a transistor BF 120 the output pulses of the TAA 790 can be used to drive a line output tube.

The positive supply voltage is connected via series resistors to pins 2 and 13, the negative pole to ground pin 14. A filtered voltage (filtering network *R13, C8*) is required at pin 2. The voltage at pin 13 is stabilized by an internal Zener diode.

The input video signal (pos. sync pulses) is fed to pin 9 of the IC through an *RC* coupling network *C1, C2, R1, R2*. The base of the noise suppression stage is connected to pin 8 and is held “ON” by a current supplied by resistor *R5*. If noise suppression is required, an additional inverted video signal (neg. sync pulses) must be applied to pin 8.

The sync separator output is connected to pin 7. The separated pulses are available at resistor *R6*. They are then fed to the integrating network of the vertical amplifier and through coupling filter *C3, C4, C12, R4, R6*, to pin 3 of the phase comparator (reference frequency input). The comparison signal is internally fed from the oscillator to the phase comparator.

The oscillator capacitor *C7* (Styroflex type with ± 5 % tolerance) is connected to pin 11. A DC control voltage is needed at pin 12. This control voltage is adjustable by means of potentiometer P. It is obtained from the stabilized voltage at pin 13 by means of the voltage divider *R8, P, R9* and *R10*. The control signal synchronizing the oscillator is supplied from the phase comparator through pin 4. It is fed into the voltage divider at junction point *R9, R10*. From pin 1 the output signal of the oscillator is available as a rectangular pulse signal. This signal serves to drive the horizontal amplifier.

Pin 6 is intended for the adjustment of the phase shift t_v (see Figs. 4 . . . 7) and accordingly the horizontal position of the image on the screen of the picture tube. A resistor connected between pins 6 and 13 increases t_v and displaces the image to the right (see Fig. 5). A resistor connected between pins 6 and 14, displaces the image to the left, t_v becoming smaller or negative (see Fig. 6). A change in t_v causes the same change in the output pulse duration, t_I.

The switching stage has an auxiliary function. When the two signals supplied by the sync separator and the oscillator respectively are in synchronism, pin 10 is switched from high to very low resistance to ground. Thus an additional *RC* network *R7*, *C9* is paralleled to the smoothing capacitor *C10*, so enlarging the filter time constant. By this means the control signal generated in the phase comparator is smoothed, so providing noise-free operation in the synchronous state.

5 W Audio Power Amplifier

The TBA 800 C is a monolithic integrated class B push-pull power amplifier in a 12-lead dual in-line plastic package with leads specially formed to facilitate automatic insertion of the device in suitable punched printed circuit boards. The external cooling tabs enable 2.5 W power output to be achieved without external heat sink and 5 W power output using a small area of the printed circuit board copper as a heat sink.

The TBA 800 C provides 5 W power output at 24 V supply voltage 16 Ω load impedance and works with a wide range of supply voltage (5 to 30 V). It gives high output current (up to 1 A), high efficiency (70 % at 4 W output), very low harmonic distortion and no cross-over distortion.

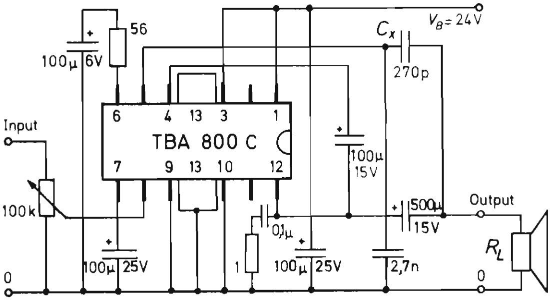
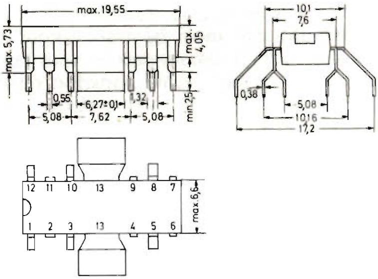


Fig. 1: Test circuit

Fig. 2:
TBA 800 C in dual in-line plastic package

Weight approx. 1.5 g
Dimensions in mm



All voltages are referred to pins 9 and 10.

Maximum Ratings

Supply voltage	V_1, V_3	30	V
Output peak current non repetitive	I_{12}	2	A
repetitive	I_{12}	1.5	A
Power dissipation at T_{amb} = 70 °C	P_{tot}	1	W
at T_{tab} = 75 °C	P_{tot}	5	W
Junction temperature	T_j	150	°C
Storage temperature range	T_S	−25 . . . +85	°C

Characteristics
for V_B = 24 V, R_L = 16 Ω, f = 1 kHz, T_{amb} = 25 °C in the test circuit Fig. 1

Quiescent output voltage	V_{12}	12 (11 . . . 13)	V
Quiescent current consumption	I_1+I_3	9 (< 20)	mA
Bias current	I_8	< 5	µA
Output power at k = 10 %	P_o	> 4.4	W
Input sensitivity for P_o = 5 W	V_8	80	mV
Input resistance	r_8	5 (> 1)	MΩ
Frequency response (− 3 dB)	$f_{3\,dB}$	40 . . . 20 000	Hz
Distortion at 0.05 . . . 2.5 W	k	0.5	%
Voltage gain with feedback as shown in Fig. 1	G_v	42 (39 . . . 45)	dB
Open loop voltage gain	G_v	80	dB
Input noise	V_r	5	µV
Efficiency at P_o = 4 W	η	70	%
Thermal resistance Junction to ambient air	R_{thA}	70	°C/W
Junction to tab	R_{thT}	12	°C/W

Fig. 3:
Output power
versus supply voltage
in the test circuit Fig. 1

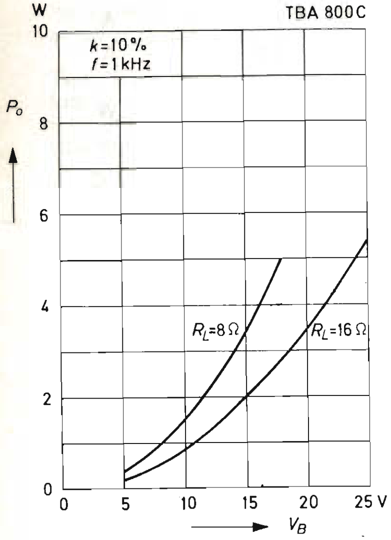


Fig. 4:
Distortion factor
versus output power
in the test circuit Fig. 1

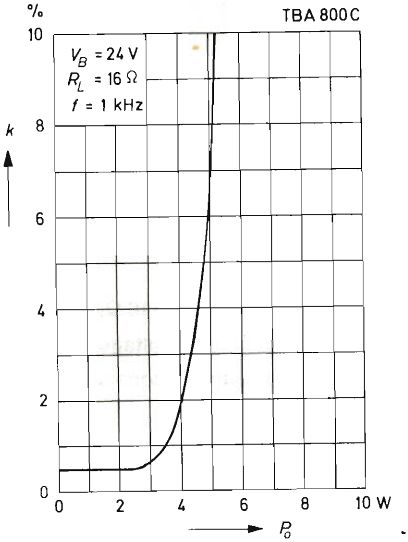


Fig. 5:
Distortion factor versus frequency
in the test circuit Fig. 1

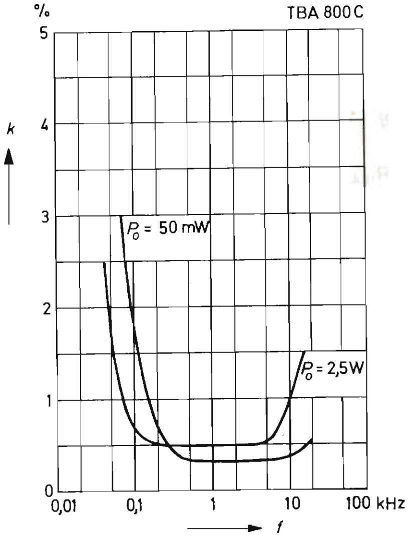


Fig. 6:
Frequency response
in the test circuit Fig. 1

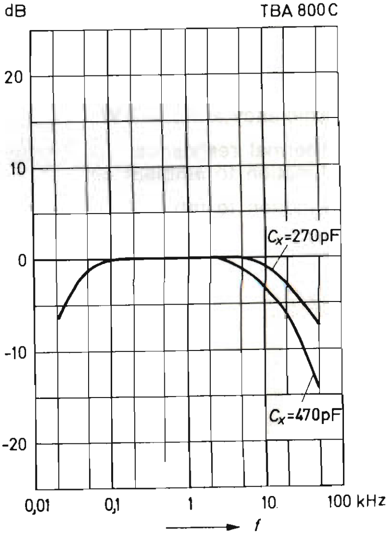


Fig. 7:
Power dissipation and efficiency versus output power in the test circuit Fig. 1

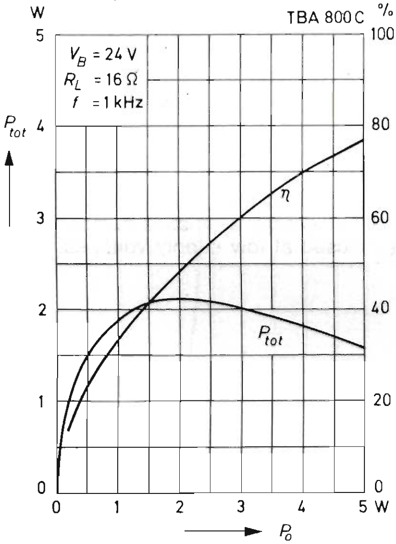


Fig. 8:
Quiescent current consumption versus supply voltage in the test circuit Fig. 1

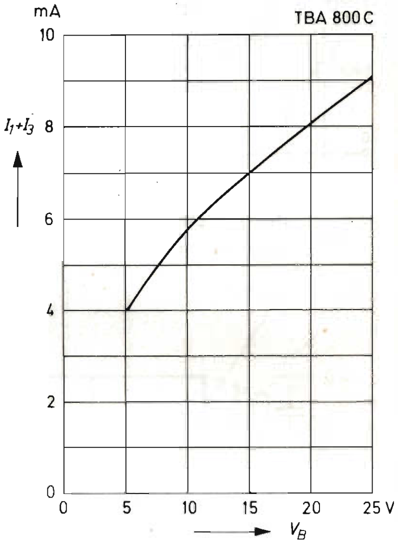


Fig. 9:
Permissible power dissipation versus side length of two identical square copper areas on a p.c. board for $T_{amb} < 55$ °C; see Fig. 16

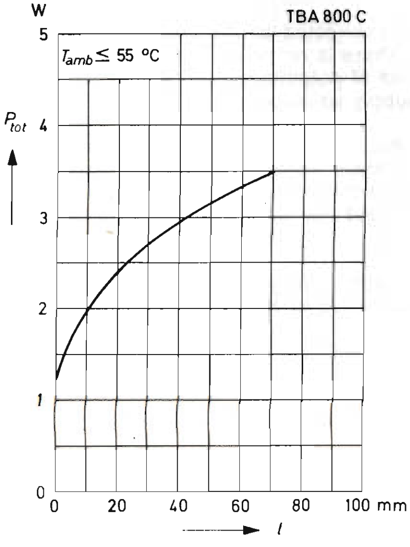
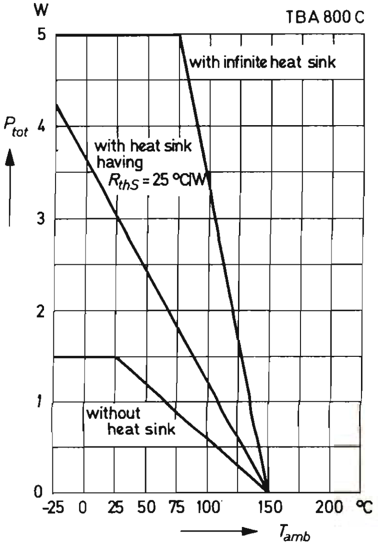


Fig. 10:
Permissible power dissipation versus ambient temperature



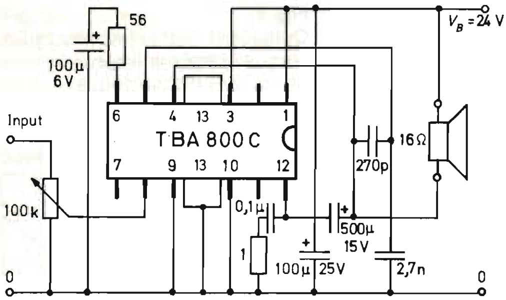


Fig. 11: Operating circuit with the load connected to the positive pole of the supply voltage. This configuration entails a smaller number of external components and can be used at low supply voltages.

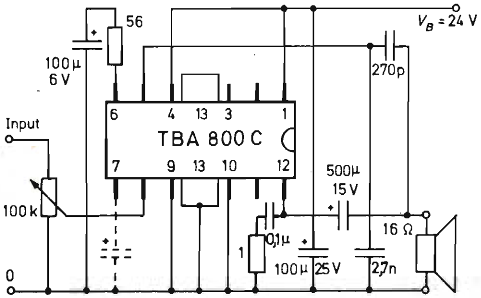


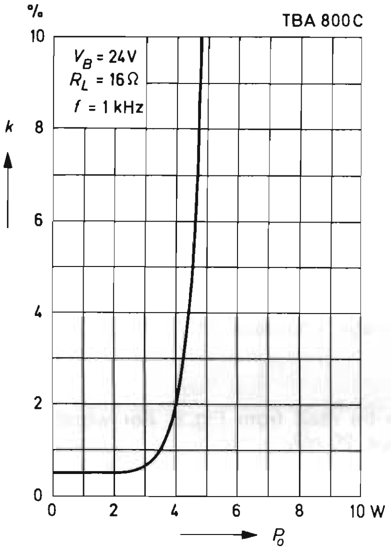
Fig. 12: Operating circuit with the load connected to the negative pole of the supply voltage (ground). There is no bootstrap connection and hence there is a greater loss of potential output swing. This circuit is only for use at high supply voltages.

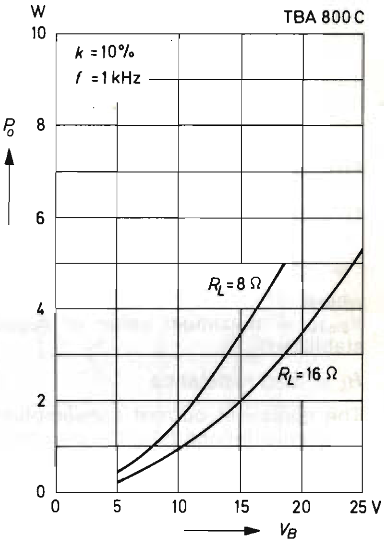
In the absence of "bootstrap", the reduction in the upper part of the wave is greater than in the lower part. If pin 3 is left open circuit, this automatically inserts two integrated diodes (internally connected to pin 3, see Fig. 17) and this enables a symmetrical wave to be obtained at the output.

For this circuit an excellent supply voltage ripple rejection is obtained by connecting a capacitor (10 to 100 µF, 25 V) between pin 7 and ground.

Fig. 13:
Distortion factor versus output power in the circuit Fig. 12

Fig. 14:
Output power versus supply voltage in the circuit Fig. 12





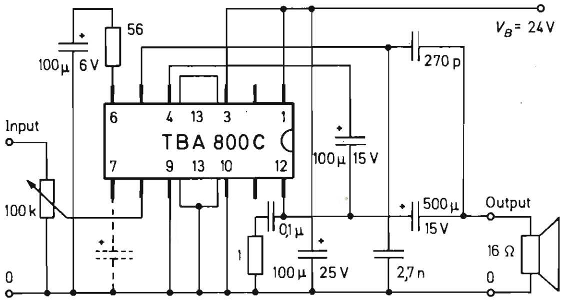


Fig. 15: Operating circuit. The bootstrap capacitor of 100 µF between pins 12 and 4 enables the same electrical characteristics as circuit of Fig. 1 to be achieved. For low supply voltage operation, e. g. 9 to 14 V, a 150 Ω resistor is connected between pins 1 and 4.

For this circuit an excellent supply voltage ripple rejection is obtained by connecting a capacitor (10 to 100 µF, 25 V) between pin 7 and ground.

Mounting Instructions

The tabs on the TBA 800 C can be used to conduct away the heat generated in the integrated circuit so that the junction temperature does not exceed the permissible maximum temperature of 150 °C. At an output power up to 2.5 W the tabs themselves are sufficient large. At higher output power these tabs have to be connected to additional heatsinks. These may be copper foil areas on the p. c. board soldered to the tabs as shown in Fig. 16. The required side length of two identical square heat sink areas for an ambient temperature of T_{amb} = 55 °C is shown in Fig. 9. The thickness of the copper layer 35 µm.

Procedure to calculate the area of copper needed

1) Calculate maximum power to be dissipated

$$P_{tot} = 0.4 \cdot \frac{(V_{Bmax})^2}{8 \cdot R_L} + V_{Bmax} \cdot \text{Quiescent current consumption}$$

where

V_{Bmax} = maximum value of supply voltage (increase by 10 % if not stabilized)

R_L = load resistance

The quiescent current consumption can be read from Fig. 8. For worst case calculations take the maximum value, 20 mA.

2) Fig. 16 gives the required side length l of one square copper foil area.

Examples

a) V_B = 24 V not stabilized, R_L = 16 Ω

$$P_{tot} = 0.4 \cdot \frac{(24 + 2.4)^2}{8 \cdot 16} + (24 + 2.4) \cdot 20 \cdot 10^{-3} = 2.6\ \text{W}$$

Fig. 9 gives a side length of l = 25 mm approximately.

For geometries different from the one of Fig. 16 note that copper areas near the tabs have better efficiency as regards power dissipation. Therefore additional safety factors must be added for worst case designs.

b) V_B = 12 V stabilized, R_L = 8 Ω

$$P_{tot} = 0.4 \cdot \frac{12^2}{8 \cdot 8} + 12 \cdot 20 \cdot 10^{-3} = 1\ \text{W}$$

Fig. 9 shows that no heat sink is required if $T_{amb} \leq 55$ °C.

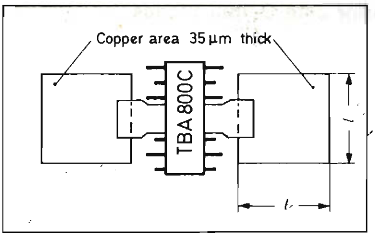


Fig. 16: Copper foil layer on the p. c. board as an additional heat sink

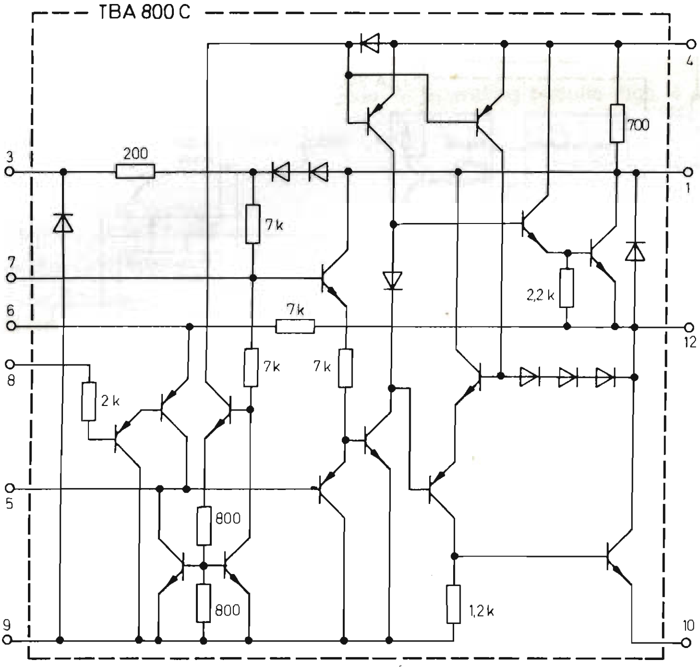


Fig. 17: Internal circuitry

Controlled Pulse Generator for Thyristor Line Output Stages

Monolithic integrated circuit for pulse separation and line synchronization in TV receivers with thyristor line output stage.

The TBA 940 is an advanced version of the TAA 790. It comprises the sync separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity, the line oscillator with frequency range limiter, a phase control circuit and the output stage.

It delivers a prepared frame sync pulse for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration few external components are needed.

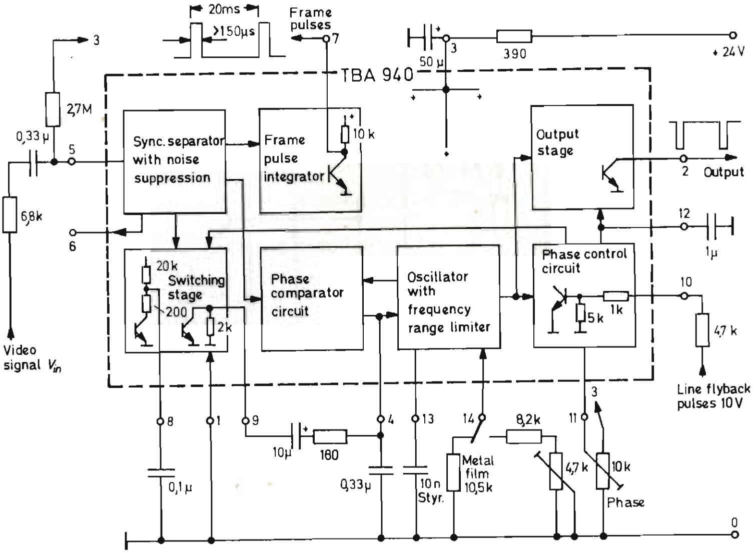
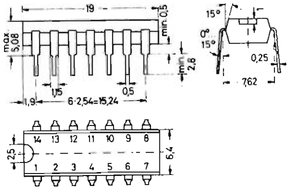


Fig. 1: Block diagram and test circuit

Fig. 2:
TBA 940 in dual in-line (Dil) plastic TO-116 package
20 A 14 according to DIN 41 866

Weight approx. 1.1 g
Dimensions in mm



All voltages are referred to pin 1.

Maximum Ratings

Supply current (see Fig. 6)	I_3	45	mA
Input current	I_5	2	mA
Input voltage	V_5	–6	V
Output current	I_2	22	mA
Output voltage	V_2	12	V
Switch-over current for video recording operation	I_8	5	mA
Flyback peak pulse current	I_{10}	5	mA
Phase correction voltage	V_{11}	0 . . . V_3	
Ambient temperature	T_{amb}	60	°C

Recommended Operating Conditions for operating circuits Figs. 4 and 5

Input current during the sync pulse	I_5	> 5	µA
BAS input signal	$V_{in\,pp}$	3 (1 . . . 6)	V
Input current during the line flyback pulse	I_{10}	0.2 . . . 2	mA
Switch-over current	I_8	> 2	mA
Time difference between the output pulse at pin 2 and the flyback pulse at pin 10	t_d	< 20	µs
Current consumption (see Fig. 6)	I_3	≤ 45	mA
Ambient operating temp. range	T_{amb}	0 . . . 60	°C

Characteristics
for $T_{amb} = 25$ °C, $f_o = 15\,625$ Hz [1]) in the test circuit Fig. 1

Amplitude of the frame pulse	V_7	> 8	V
Frame pulse duration	t_7	> 150	µs
Output resistance at pin 7 (high state)	$R_{out\,7}$	10 (7.5 . . . 13)	kΩ
Amplitude of the complete sync signal	V_6	> 8	V
Output resistance at pin 6	$R_{out\,6}$	2.5 . . . 4.5	kΩ
Output pulse duration	t_2	4 . . . 8	µs
Residual output voltage at $I_2 = 20$ mA	$V_{2\,res}$	< 0.55	V

[1]) By modification of the frequency determining network at pins 13 and 14 the TBA 940 can also be used for other line frequencies.

Oscillator frequency for $C_{13/1} = 10$ nF, $R_{14/1} = 10.5$ kΩ	f_o	15 625 ± 1562	Hz
Frequency pull-in range	$\pm \Delta f_F$	400 . . . 1000	Hz
Frequency holding range	$\pm \Delta f_H$	400 . . . 1000	Hz
Slope of phase comparator control loop	df_o/dt_d	2	kHz/µs
Gain of phase control	dt_d/dt_p	20	
Phase shift between leading edge of BAS signal and line flyback pulse[1]) at $t_5 = 4.7$ µs, $t_{10} = 12$ µs, $t_s = 5$ µs, pin 11 open circuit, see Fig. 3	t_v	−1 . . . +3.5	µs

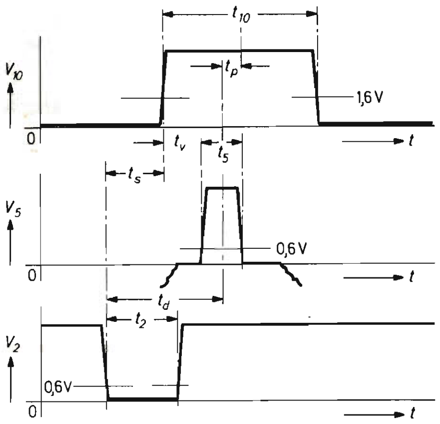


Fig. 3: Phase relations of the TBA 940.

[1]) The limited flyback pulse should overlap the BAS signal sync pulse on both edges.

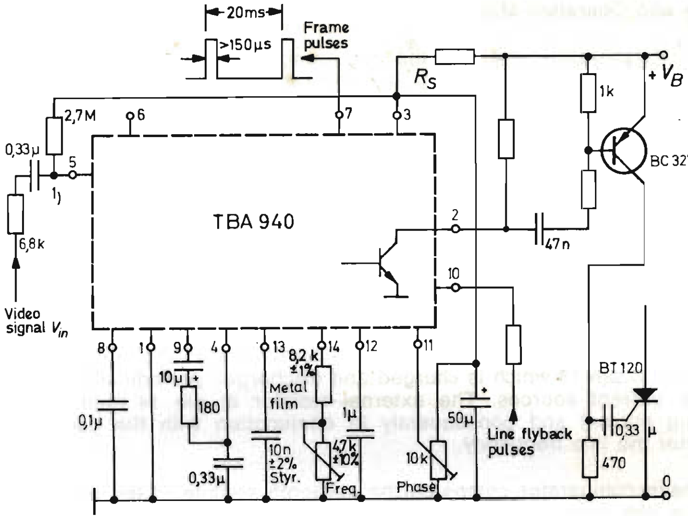


Fig. 4: Operating circuit

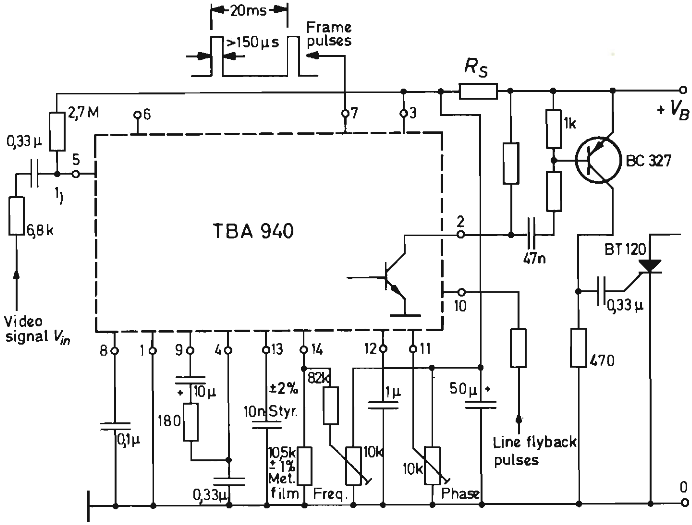


Fig. 5: Another possibility for line frequency adjustment

[1]) Input circuitry must be optimized.

Design and Operation Mode

The sync separator separates the synchronizing pulses from the composite video signal (BAS signal). The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The *RC* network hitherto required between sync separator and frame oscillator is no longer needed. Since the frame sync pulse duration at pin 7 is subject to production spreads it is recommended to use the leading edge of this pulse for triggering.

The frequency of the line oscillator is determined by a 10 nF Styroflex capacitor at pin 13 which is charged and discharged periodically by two internal current sources. The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulses. Simultaneously an AFC voltage is generated which influences the oscillator frequencv. A frequency range limiter restricts the frequency holding range.

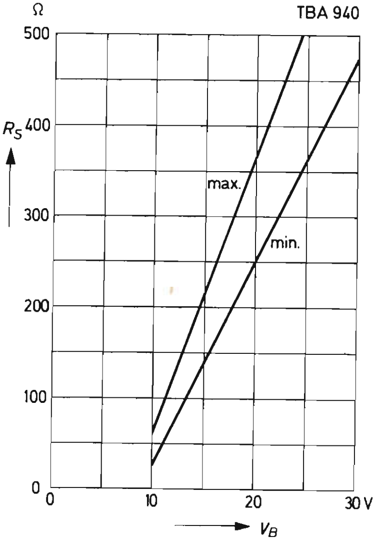
The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e. g. due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync pulse on both edges (see Fig. 3).

The switching stage has an auxiliary function. When the two signals supplied by the sync separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin 9. Thus the time constant of the filter network at pin 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50 Hz. This arrangement ensures disturbance-free operation.

For video recording operation this automatic switchover can be blocked by a positive current fed into pin 8, e. g. via a resistor connected to pin 3. It may also be useful to connect a resistor of about 680 Ω or 1 kΩ between pin 9 and ground. The capacitor at pin 4 may be lowered, e. g. to 0.1 μF. This alterations do not significantly influence the normal operation of the IC and thus do not need to be switched.

The output stage delivers at pin 2 output pulses of duration and polarity suitable for driving the line driver stage. If the supply voltage goes down (e. g. by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to $V_3 = 4$ V and shuts off when V_3 falls below 4 V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V_3 reaches 4.5 V. In the range between $V_3 = 4.5$ V and full supply the shape and frequency of the output pulses are practically constant.

Fig. 6:
Graph for determining the supply series resistor R_S



Controlled Pulse Generators for Transistor Line Output Stages

Monolithic integrated circuit for pulse separation and line synchronization in TV receivers with transistor line output stage.

The TBA 950 is an advanced version of the TAA 790. It comprises the sync separator with noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity, the line oscillator with frequency range limiter, a phase control circuit and the output stage.

It delivers prepared frame sync pulses for triggering the frame oscillator. The phase comparator may be switched for video recording operation. Due to the large scale of integration few external components are needed.

The 950 is delivered in two groups having different output pulse durations. The TBA 950:F is designed for TV receivers according to the French standard.

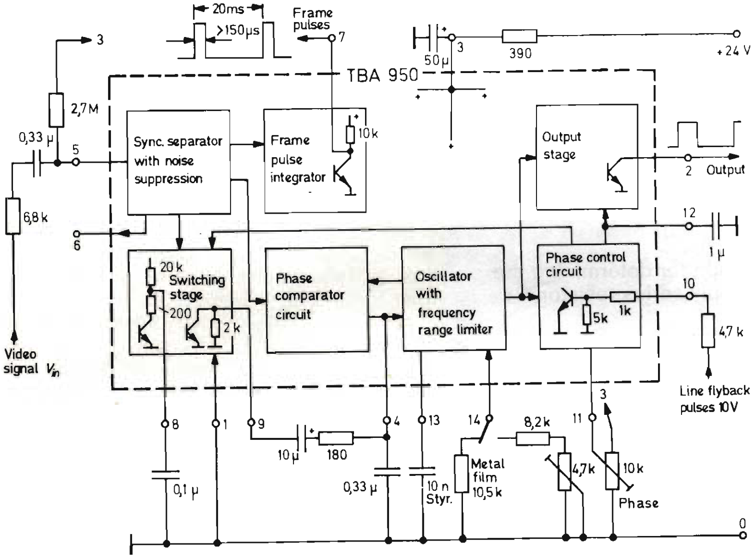
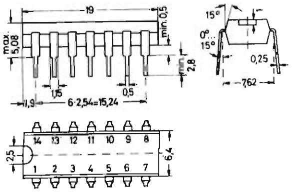


Fig. 1: Block diagram and test circuit for the TBA 950

Fig. 2:
TBA 950 in dual in-line (Dil) plastic TO-116 package
20 A 14 according to DIN 41 866

Weight approx. 1.1 g
Dimensions in mm



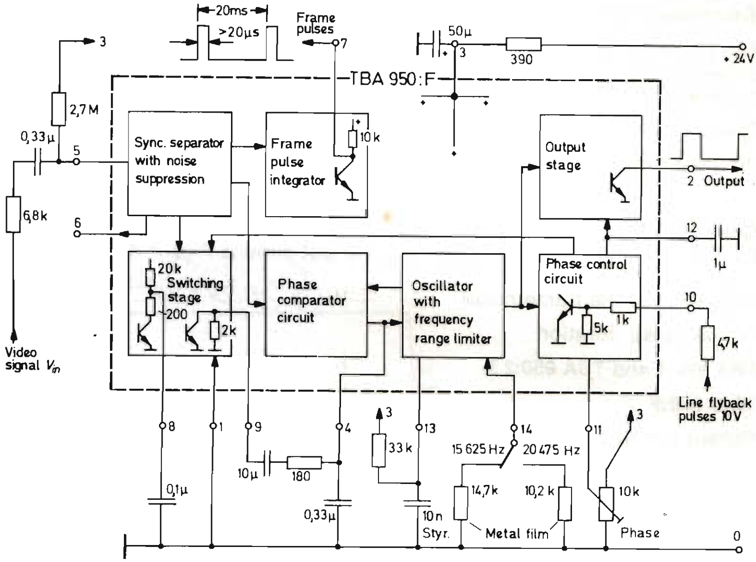


Fig. 3: Block diagram and test circuit for the TBA 950:F

All voltages are referred to pin 1.

Maximum Ratings

Supply current (see Fig. 8)	I_3	45	mA
Input current	I_5	2	mA
Input voltage	V_5	−6	V
Output current	I_2	22	mA
Output voltage	V_2	12	V
Switch-over current for video recording operation	I_8	5	mA
Flyback peak pulse current	I_{10}	5	mA
Phase correction voltage	V_{11}	$0 \ldots V_3$	
Ambient temperature	T_{amb}	60	°C

Recommended Operating Conditions for operating circuits Figs. 5 to 7

Input current during the sync pulse	I_5	> 5	µA
BAS input signal	$V_{in\,pp}$	3 (1 . . . 6)	V
Input current during the line flyback pulse	I_{10}	0.2 . . . 2	mA

Switch-over current	I_8	> 2	mA
Time difference between the output pulse at pin 2 and the line flyback pulse at pin 10	t_d	< 20	µs
Current consumption (see Fig. 8)	I_3	≤ 45	mA
Ambient operating temp. range	T_{amb}	0 . . . 60	°C

Characteristics
for T_{amb} = 25 °C, f_o = 15 625 Hz [1]) in the test circuits Figs. 1 and 3

Amplitude of the frame pulse	V_7	> 8	V
Frame pulse duration			
TBA 950:1 and TBA 950:2 X	t_7	> 150	µs
TBA 950:F	t_7	> 20	µs
Output resistance at pin 7 (high state)	$R_{out\,7}$	10 (7.5 . . . 13)	kΩ
Amplitude of the complete sync signal	V_6	> 8	V
Output resistance at pin 6	$R_{out\,6}$	2.5 . . . 4.5	kΩ
Output pulse duration			
TBA 950:1	t_2	22 . . . 26	µs
TBA 950:2 X	t_2	25 . . . 28	µs
TBA 950:F	t_2	25 . . . 30	µs
Residual output voltage at I_2 = 20 mA	$V_{2\,res}$	< 0.55	V
Oscillator frequency for $C_{13/1}$ = 10 nF, $R_{14/1}$ = 10.5 kΩ	f_o	15 625 ± 1562	Hz
Frequency pull-in range	$\pm \Delta f_F$	400 . . . 1000	Hz
Frequency holding range	$\pm \Delta f_H$	400 . . . 1000	Hz
Slope of phase comparator control loop	df_o/dt_d	2	kHz/µs
Gain of phase control	dt_d/dt_p	20	
Phase shift between leading edge of BAS signal and line flyback pulse [2]) at t_5 = 4.7 µs, t_{10} = 12 µs, t_s = 5 µs, pin 11 open circuit, see Fig. 4	t_v	− 1 . . . + 3.5	µs

[1]) By modification of the frequency determining network at pins 13 and 14 these integrated circuits can also be used for other line frequencies.

[2]) The limited flyback pulse should overlap the BAS signal sync pulse on both edges.

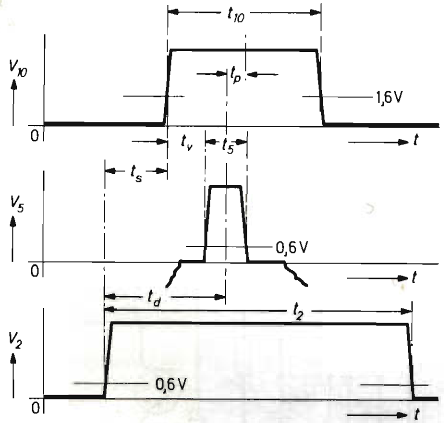


Fig. 4: Phase relations of the TBA 950.

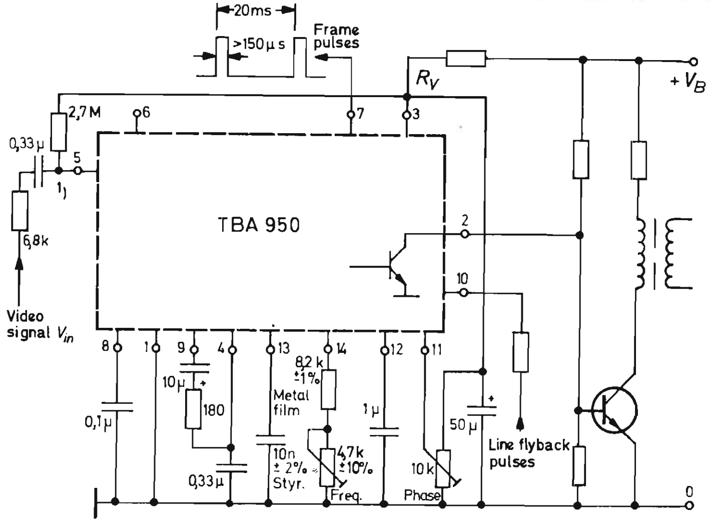


Fig. 5: Operating circuit

[1]) Input circuitry must be optimized.

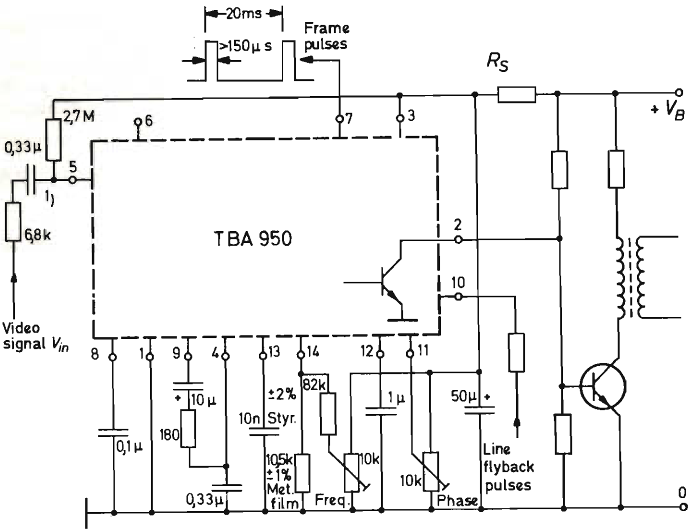


Fig. 6: Another possibility for line frequency adjustment for the TBA 950

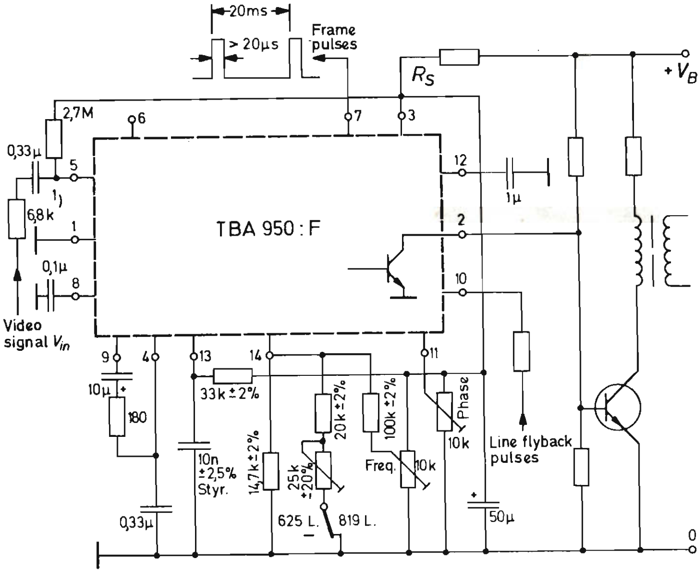


Fig. 7: Operating circuit of the TBA 950:F with line frequency changeover from 625 lines to 819 lines

1) Input circuitry must be optimized.

Design and Operation Mode

The sync separator separates the synchronizing pulses from the composite video signal (BAS signal). The noise inverter circuit, which needs no external components, in connection with an integrating and differentiating network frees the synchronizing signal from distortion and noise.

The frame sync pulse is obtained by multiple integration and limitation of the synchronizing signal, and is available at pin 7. The *RC* network hitherto required between sync separator and frame oscillator is no longer needed. Since the frame sync pulse duration at pin 7 is subject to production spreads it is recommended to use the leading edge of this pulse for triggering.

The frequency of the line oscillator is determined by a 10 nF Styroflex capacitor at pin 13 which is charged and discharged periodically by two internal current sources. The external resistor at pin 14 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulses. Simultaneously an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

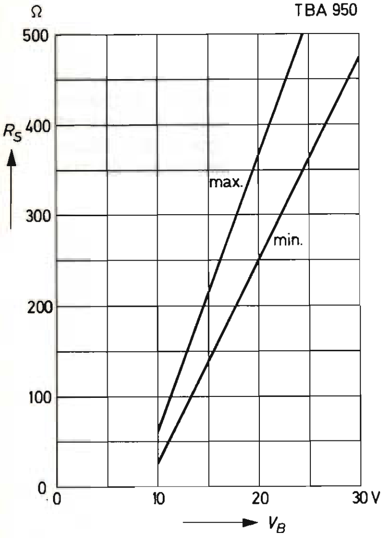
The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The correct phase position and hence the horizontal position of the picture can be adjusted by the 10 kΩ potentiometer connected to pin 11. Within the adjustable range the output pulse duration (pin 2) is constant. Any larger displacements of the picture, e. g. due to non-symmetrical picture tube, should not be corrected by the phase potentiometer, since in all cases the flyback pulse must overlap the sync pulse on both edges (see Fig. 4).

The switching stage has an auxiliary function. When the two signals supplied by the sync separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin 9. Thus the time constant of the filter network at pin 4 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state to approximately 50 Hz. This arrangement ensures disturbance-free operation.

For video recording operation this automatic switchover can be blocked by a positive current fed into pin 8, e. g. via a resistor connected to pin 3. It may also be useful to connect a resistor of about 680 Ω or 1 kΩ between pin 9 and ground. The capacitor at pin 4 may be lowered, e. g. to 0.1 µF. This alterations do not significantly influence the normal operation of the IC and thus do not need to be switched.

The output stage delivers at pin 2 output pulses of duration and polarity suitable for driving the line driver stage. If the supply voltage goes down (e.g. by switching off the mains) a built-in protection circuit ensures defined line frequency pulses down to $V_3 = 4$ V and shuts off when V_3 falls below 4 V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V_3 reaches 4.5 V. In the range between $V_3 = 4.5$ V and full supply the shape and frequency of the output pulses are practically constant.

Fig. 8:
Graph for determining the supply series resistor R_S



DC Converter

Monolithic integrated circuit designed for generating a stabilized and temperature independent tuning voltage in diode-tuned and battery-powered radio receivers the tuning voltage of which is higher than the battery voltage.

The TCA 720 comprises a blocking oscillator and a temperature compensated voltage control circuit. The operating frequency of the blocking oscillator is determined by the coil inductance and the supply voltage.

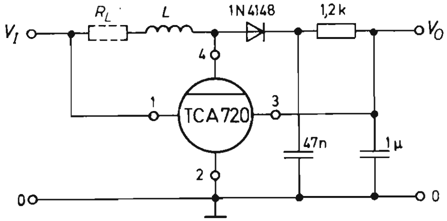
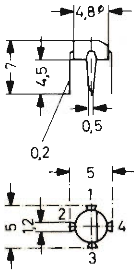


Fig. 1: Application circuit

Fig. 2:
TCA 720 in plastic package
50 B 4 according to DIN 41 867

Weight approximately 0.1 g
Dimensions in mm



All voltages are referred to pin 2.

Maximum Ratings

Supply voltage	V_1	20	V
Ambient operating temperature range	T_{amb}	– 20 . . . +70	°C
Storage temperature range	T_S	– 40 . . . +125	°C

Characteristics at L = 5 mH, R_L = 20 Ω, T_{amb} = 25 °C in the circuit Fig. 1

Output voltage	V_O	30 . . . 35	V
Supply voltage range at I_O = 1 mA	V_I	4.5 . . . 18	V
Change of the output voltage at V_I = 4.5 . . . 9 V, I_O = 1 mA	$\Delta V_O/V_O$	$6 \cdot 10^{-4}$	
at V_I = 9 . . . 18 V, I_O = 1 mA	$\Delta V_O/V_O$	$6 \cdot 10^{-4}$	
Output voltage temperature coefficient at V_I = 9 V, I_O = 1 mA	$\frac{\Delta V_O}{V_O \cdot \Delta T_{amb}}$	$\pm 8 \cdot 10^{-5}$	$°C^{-1}$
Operating frequency at V_I = 9 V	f	100	kHz
Current consumption at V_I = 4.5 V, I_O = 1 mA	I_I	14	mA
at V_I = 9 V, I_O = 1 mA	I_I	9	mA
at V_I = 18 V, I_O = 1 mA	I_I	7.5	mA

TDA 1035

Sound Channel IC for TV Receivers

The TDA 1035 is a monolithic integrated circuit containing all stages required in the sound channel of a TV receiver. It is suitable for mains as well as battery-operated receivers and is contained in a plastic package similar to TO-116, with 13 connection pins. These pins are shaped and arranged in such a way that automatic application to printed circuit boards can be carried out without difficulty. The cooling tabs projecting from the case on either side are sufficiently large for a 2 W output power without additional heat sink facilities. If these tabs are cooled further, for example by being soldered to a sufficiently large copper-clad area of the printed circuit board, an output power of up to 4 W is permissible.

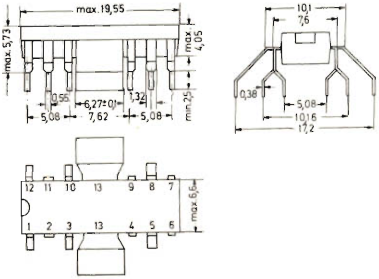
As can be seen from Figs. 2 to 4, the TDA 1035 requires only few external components. It consists of a limiting IF amplifier, a coincidence demodulator, an electronic volume control circuit and a complete AF amplifier with preamplifier, driver and output stage in series push-pull configuration. The IF section has excellent limiting properties and operates with high AM suppression. The coincidence demodulator supplies a low-distortion AF signal. For connection to a video recorder, the TDA 1035 is provided with a direct demodulator output which is not affected by the electronic volume control.

In order to receive signals from the AF output of a video recorder or from other AF signal sources, the TDA 1035 is provided with an AF input which can be influenced by the electronic volume control. A switching voltage allows the IF section to be switched off.

The output amplifier is protected against overheating. At a chip temperature of approximately 150 °C the AF voltage at the driver transistor is short-circuited.

Fig. 1:
TDA 1035 in a plastic package

Weight approx. 1.5 g
Dimensions in mm



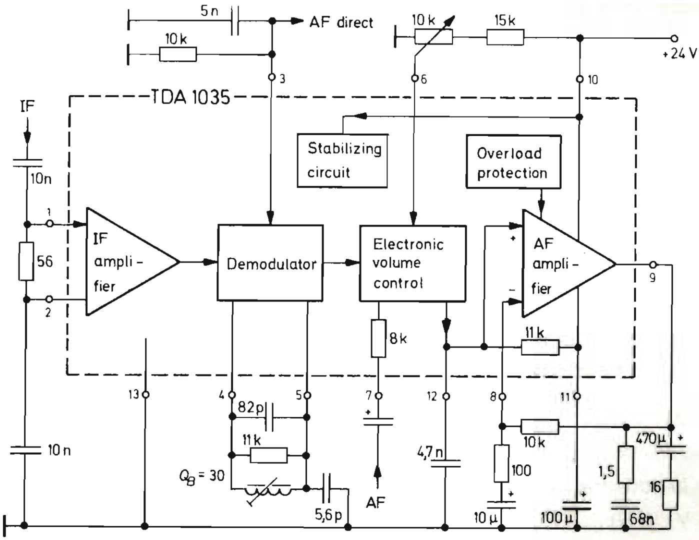


Fig. 2: Block diagram of the TDA 1035 and test circuit for the characteristics

All voltages are referred to pin 13 (cooling tabs).

Maximum Ratings

Supply voltage	V_{10}	30	V
Current consumption	I_{10}	400	mA
Input currents	I_1	1	mA
	I_4	1	mA
	I_5	1	mA
	I_6	1	mA
	I_7	1	mA
Input voltages	$V_{1/2rms}$	1	V
	$V_{7/rms}$	1	V
	V_6	0 . . . 12	V
Output current	I_{9pp}	2	A
at $V_{10} < 22$ V	I_{9pp}	2,5	A
Total power dissipation			
at T_{amb} = 70 °C	P_{tot}	1	W
at T_{tab} = 100 °C	P_{tot}	4	W
Junction temperature	T_j	150	°C
Storage temperature range	T_S	−25 . . . +100	°C

Characteristics at $V_{10} = 24$ V, $f_i = 5.5$ MHz, $f_{AF} = 1$ kHz, $\pm \Delta f = 50$ kHz, $R_L = 16\ \Omega$, figure of merit of the demodulator circuit at pins 4 and 5 $Q_B = 30$ [1]), in the test circuit Fig. 2

AF output voltage at $V_1 = 10$ mV	$V_{12\,RMS}$	0.6	V
	$V_{3\,RMS}$	1	V
AM suppression			
at $V_1 = 1$ mV, $m = 30$ %	α	40	dB
at $V_1 = 10$ mV, $m = 30$ %	α	50	dB
at $V_1 = 100$ mV, $m = 30$ %	α	40	dB
Input voltage for start of limitation	V_1	< 100	µV
Distortion factor of the AF output voltage at $V_1 = 10$ mV, $f_{AF} = 1$ kHz, $Q_B \approx 20$	k	1	%
Attenuation of the electronic volume control at $V_1 = 10$ mV, $V_6 = 0$			
broadband tested	ΔV_{12}	70	dB
tested selectively at $f = 1$ kHz	ΔV_{12}	> 75	dB
Input impedance	$Z_{1/2}$	5 kΩ || 10 pF	
Gain V_7/V_{12} [2])	G	1	
Input impedance	Z_7	8	kΩ
Distortion of V_{12} at $V_{7\,RMS} = 1$ V	k	< 3	%
Voltage gain between pins 7 and 9	$G_{7/9}$	40 [3])	dB
Open loop gain of the output amplifier	$G_{12/9}$	75	dB
Output power			
at $k = 1$ %	P_o	3	W
at $k = 10$ %	P_o	4	W
Input AC voltage for $P_o = 4$ W	V_{12}	< 0.1 [3])	V
Input resistance	$R_{12/11}$	11	kΩ
Frequency response (– 3 dB) at $P_o = 0.5$ W	$f_{3\,dB}$	40	kHz
Quiescent output voltage	V_9	9.5 . . . 13	V
DC resistance required between pins 9 and 8	$R_{9/8}$	< 10	kΩ
Onset of the temperature overload protection	T_j	150	°C
Thermal resistance			
junction to ambient air	R_{thA}	70	°/CW
junction to tab	R_{thtab}	12	°C/W

1) The load placed upon the demodulator circuit by the TDA 1035 is virtually negligible.

2) Here, the IF section is rendered inoperative by a switching voltage at pins 1 and 2; for instance, by connecting these pins to +12 V via 2.7 kΩ.

3) Gain is determined by the ratio of the negative-feedback potential divider:

$$G_{7/9} = 20 \lg \frac{R_{9/8} + R_{8/13}}{R_{8/13}}$$

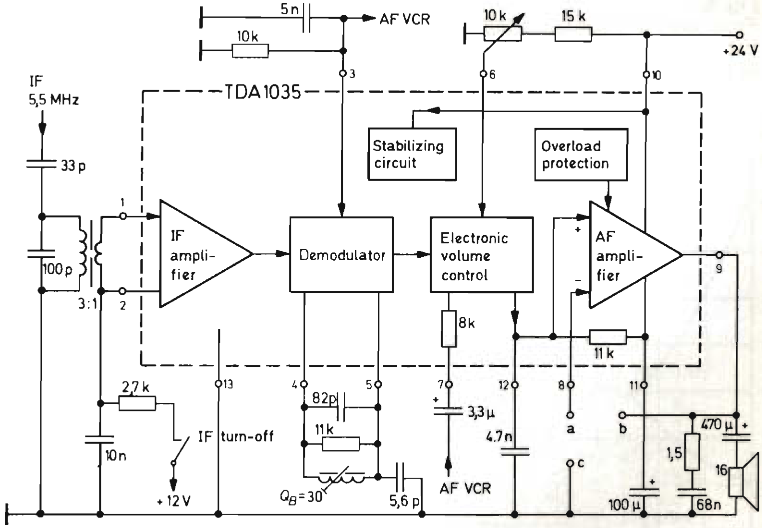


Fig. 3: Operating circuit of the TDA 1035

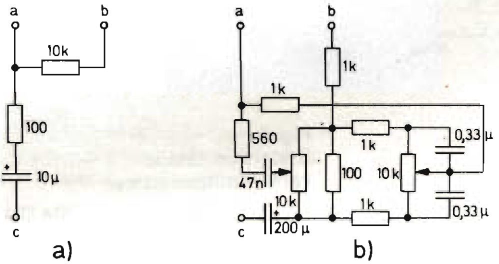


Fig. 4: Circuit detail between points a, b and c of the operation circuit above
a) without tone control network (linear frequency response)
b) with tone control network (frequency response see Fig. 6)

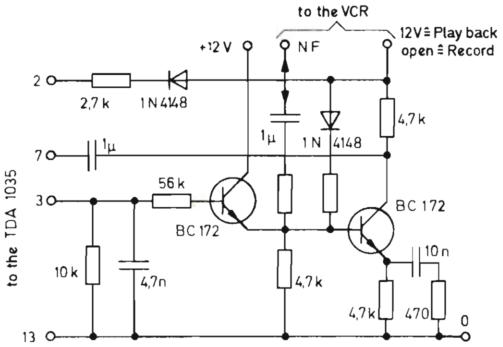


Fig. 5: Auxiliary circuit for connecting a video recorder

Fig. 6:
Frequency response of the tone control network shown in Fig. 4b

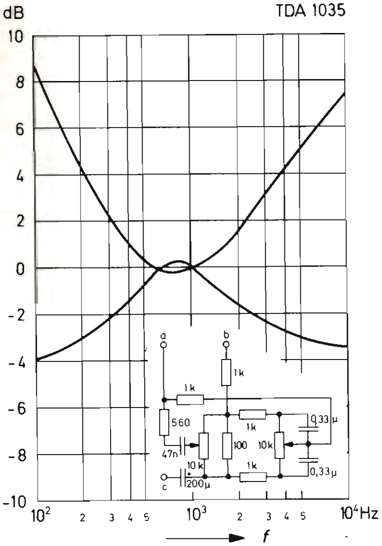


Fig. 7:
Characteristic of the electronic volume control

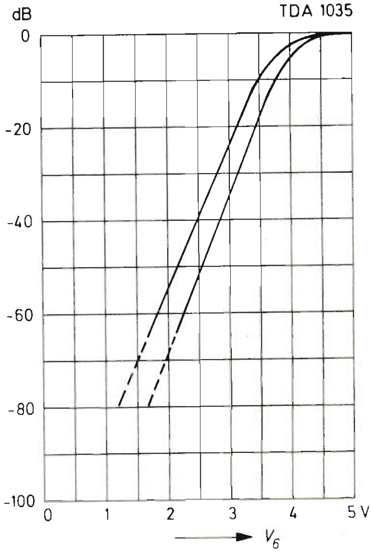


Fig. 8:
Obtainable output power versus supply voltage

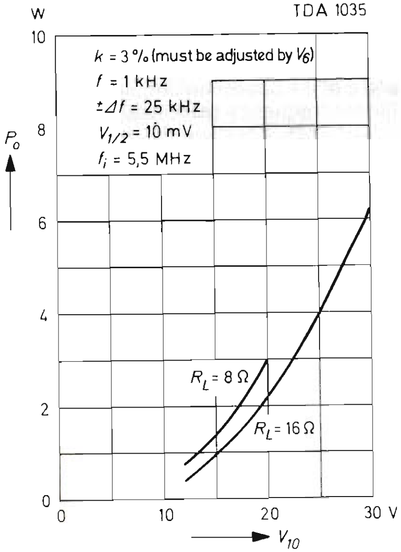


Fig. 9:
Distortion factor versus output power

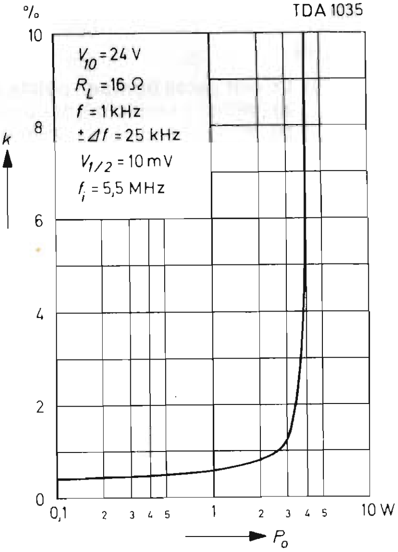


Fig. 10:
Distortion factor versus detuning of the circuit at pins 4 and 5

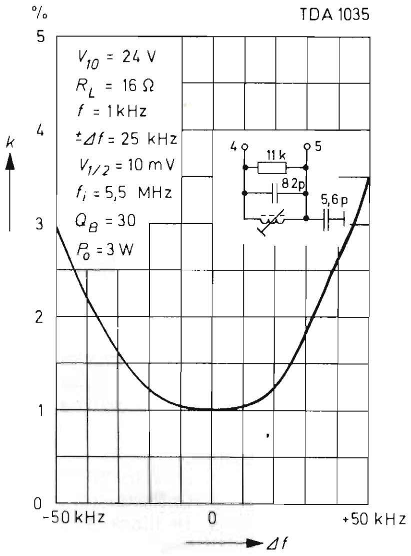


Fig. 11:
Frequency response of the AF amplifier between pins 7 and 9

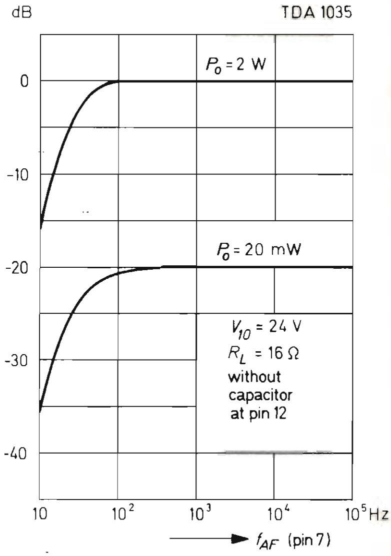
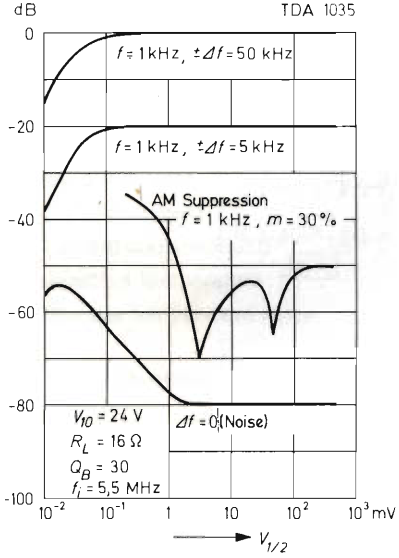


Fig. 12:
AF output level, AM suppression and unweighted signal-to-noise ratio versus input voltage



Frame Scan Circuits for TV Receivers

The TDA 1044 is a monolithic integrated circuit containing all stages for the vertical deflection of 110° black and white TV receivers. The TDA 1044 F is intended for use in color TV receivers.

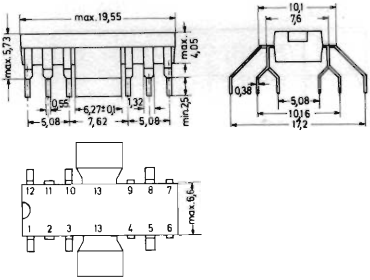
Both types comprise a linear sawtooth generator that can be synchronized with positive or negative pulses. The sawtooth generator receives its supply voltage separately via pin 12. By varying this supply voltage the amplitude of the sawtooth may be altered, so that a frame height control, e. g. coupled with the line width amplitude, may be realized. The internal geometric correction circuit, which can be matched to different screen radii by external resistors, does not require any external *RC* network and ensures tangential correction of the deflection current.

The integrated output amplifier of the TDA 1044 controls the deflection current and an integrated flyback booster circuit ensures low power dissipation of the device. The deflection current in color TV sets is controlled by a complementary pair of power transistors connected to the output of the TDA 1044 F. A negative feedback whose voltage is proportional to the deflection current ensures proportionality between sawtooth voltage and deflection current. In this way temperature dependent variations of the deflection coil resistance cannot affect the frame height and the NTC resistor hitherto connected in series with the deflection coil can be omitted.

The TDA 1044 operates within a supply voltage range of 11 V to 27 V. When operating the TDA 1044 F in connection with two power transistors (see Fig. 5) the supply voltage may be raised up to 42 V. In black and white TV receivers pin 6 of the TDA 1044 supplies positive blanking pulses with an amplitude of max. 20 V. In color TV receivers the TDA 1044 F supplies at pin 6 positive and at pin 7 negative blanking pulses.

Fig. 1:
TDA 1044 and TDA 1044 F in plastic package

Weight approximately 1.5 g
Dimensions in mm



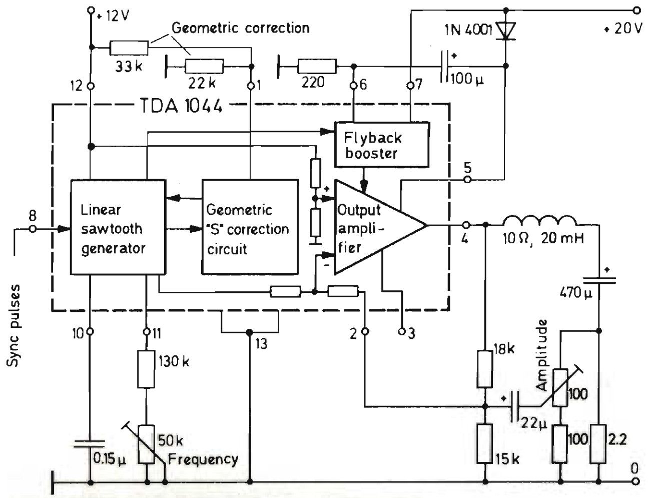


Fig. 2: Block diagram and test circuit of the TDA 1044 and the TDA 1044 F

All voltages are referred to pin 13 (cooling tabs).

Maximum Ratings

Supply voltages	V_{12}	22	V
TDA 1044 operated with flyback booster	V_5	27 [1])	V
	V_7	30	V
TDA 1044 F flyback booster circuit	V_5	42	V
used for blanking	V_7	42	V
Input voltage	V_8	– 6	V
Input current	I_8	2	mA
Output current	I_{4pp}	1	A
Flyback current	I_6	0.5	A
Current consumption	I_7+I_5	300	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_S	– 25 . . . +100	°C

Characteristics at T_{amb} = 25 °C in the test circuit Fig. 2, deflection unit 10 Ω, 20 mH

Current consumption	I_5+I_7	140	mA
	I_{12}	12	mA

[1]) during flyback pulse: 58 V

Adjustment range of deflection current	I_{4pp}	0.4 . . . 0.9	A
Flyback duration	t_{fly}	1	ms
Input impedance	$r_{8/13}$	10	kΩ
Frequency of the sawtooth generator at $R_{11/13} > 50$ kΩ	f_B	$\frac{1.6}{R_{11/13} \cdot C_{10/13}}$	
Adjustment range of the sawtooth generator	$\Delta f_B/f_B$	10	%
DC voltage at pin 11	V_{11}	9.7	V
DC current at pin 11 at $C_{10/13} = 0.15$ µF, $f_B = 50$ Hz	$-I_{11}$	45	µA
Required sync pulse amplitude at pin 8 with positive sync signal	V_8	1 . . . 10	V
with negative sync signal	V_8	− 1.3 . . . − 6	V
Geometric distortion related to standard picture tube and standard deflection unit [1])	$\Delta_{I/I}$	3	%

Recommended Operating Conditions
for the circuit shown in Fig. 3, deflection unit 10 Ω, 20 mH

Supply voltages	V_7	22	V
	V_{12}	12	V
Amplitude of positive sync pulses	V_8	8	V
Operating ambient temperature range	T_{amb}	0 . . . 60	°C
Thermal resistance of the copper-clad area soldered to the cooling tabs	R_{thS}	15	°C/W

[1]) Tangent correction can be made adjustable by potentiometers. The curvature of the deflection current S-curve may be changed by a series resistor connected to pin 1. The DC voltage at pin 1 is responsible for the up/down correction. This voltage derives from the supply voltage V_{12} and the divider ratio of the voltage divider at pin 12 and pin 1. If fixed resistors are used a ratio of approximately 1.45 for $R_{12/1}$ to $R_{1/13}$ should be observed.

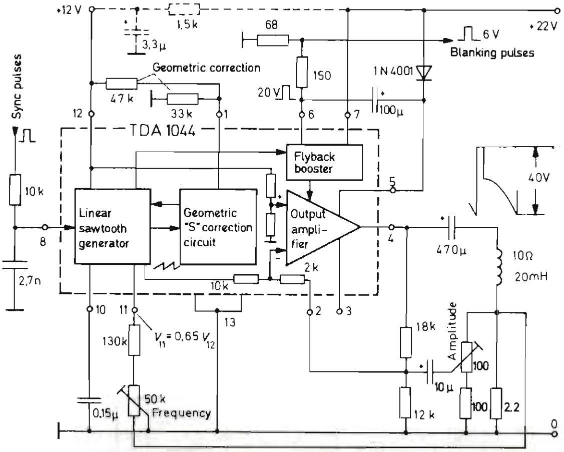


Fig. 3:
Application circuit for the TDA 1044 in black and white TV receivers

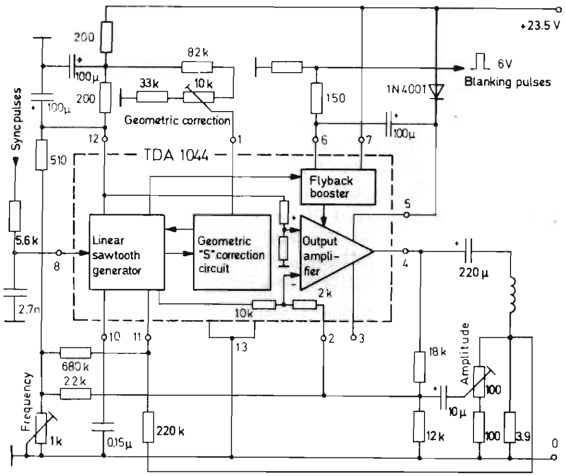


Fig. 4:
Application circuit for the TDA 1044 in black and white TV receivers showing a more extended frequency adjustment circuit. This ensures a constant vertical deflection current during any adjustment of the "Frequency" potentiometer.

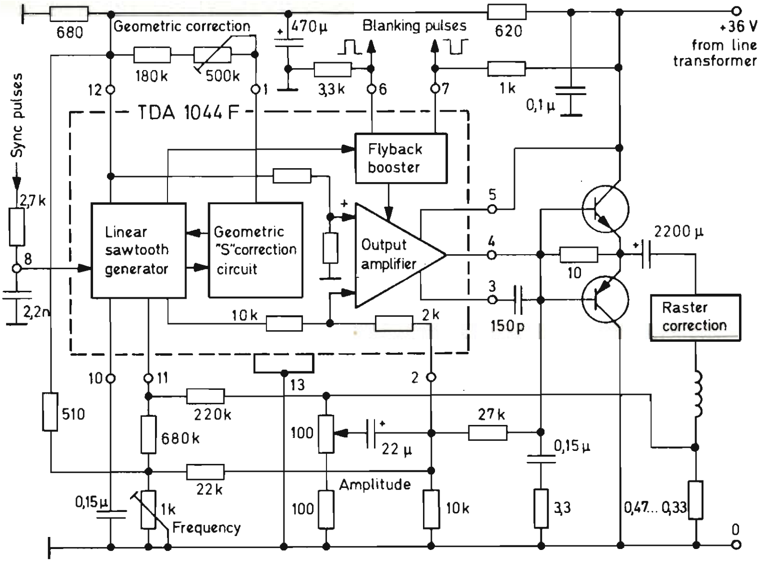


Fig. 5:
Application circuit for the TDA 1044 F in color TV receivers. The geometric correction circuit is designed for picture tubes type 20 AX and must be modified for different types. The picture height is not influenced by the adjustment of the "Frequency" potentiometer. The duration of the blanking pulses is equal to the flyback duration and therefore depending on resistance and inductance of the deflection coil. The 150 pF capacitor at pin 3 and pin 4 and also the Boucherot circuit 0.15 µF/3.3 Ω at pin 4 and GND prevent any parasitic oscillation of the output amplifier. Dimensioning depends on the relation *L*/*R* of the vertical deflection coil. The higher this relation the more compensation (more capacitance and less resistance) is required. Both compensations are not required with usual black and white deflections coils.

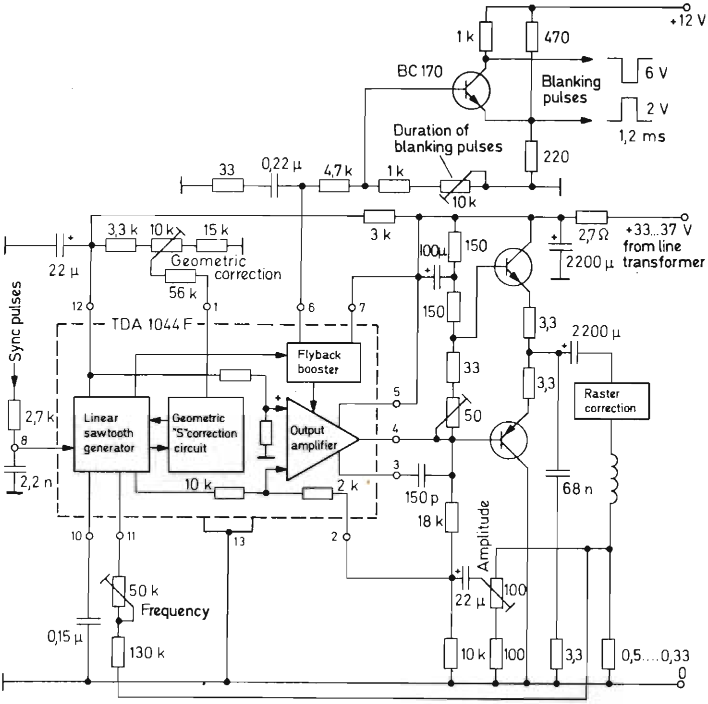


Fig. 6:
Application circuit for the TDA 1044 F in color TV receivers. The geometric correction circuit is designed for picture tubes type 20 AX and must be modified for different types. For the compensation network at pin 3 and the output the legend of Fig. 5 is also valid. A pulse shaper containing a transistor BC 170 is connected to pin 6. This circuit ensures a constant duration of the blanking pulses (approximately 1.2 ms) independent of the flyback duration and the *L*/*R* relation of the vertical deflection coil.

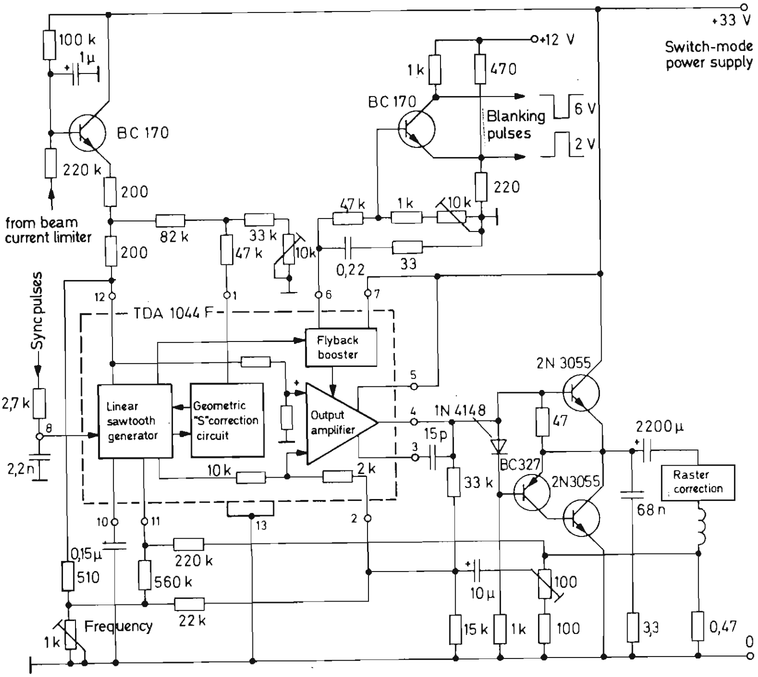


Fig. 7:
Application circuit for the TDA 1044 F in color TV receivers. The geometric correction circuit is designed for in-line picture tubes and must be modified for different types. For the compensation network at pin 5 and at the output the legend of Fig. 5 is also valid. A pulse shaper as described in the legend of Fig. 6 is connected to pin 6. Adjustment of the "Frequency" potentiometer does not influence the picture height. Via a transistor BC 170 the beam current limiter influences the supply voltage of the sawtooth generator at pin 12 and subsequently the picture heigh. Higher beam current results in a lower high-tension and enlarged picture (at constant deflection current). Reducing the oscillator amplitude via the supply voltage at pin 12 keeps constant the picture height.

PIN Diode π Network

The TDA 1053 comprises in one plastic package three silicon planar PIN diodes connected to form a π network and serves for the electronic amplitude control of the input signals of TV tuners and antenna branching amplifiers in the 40 . . . 1000 MHz range. Both, its input and its output impedances remain constant over the entire control range.

The TDA 1053 is normally supplied with vertical leads, indicated by an additional "A" to the type designation. Upon special request it is also available with horizontal leads, add suffix "B" to the type No. The ratings stated overleaf apply to devices with vertical leads.

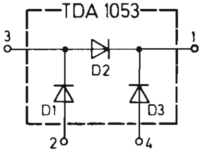


Fig. 1: Internal circuit of the TDA 1053

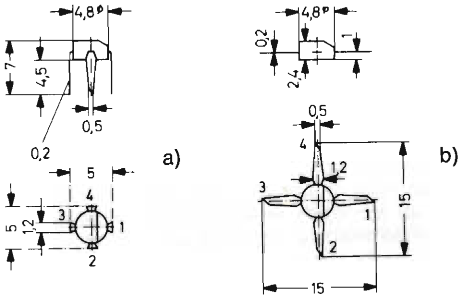


Fig. 2: TDA 1053 in plastic package 50 B 4 according to DIN 41 867
a) with vertical leads
b) with horizontal leads

Weight approximately 0.1 g   Dimensions in mm

Maximum Ratings of individual Diodes

Reverse voltage	V_R	30	V
Forward current at T_{amb} = 25 °C	I_F	50	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_S	– 55 . . . +125	°C

Maximum Ratings of the π Network

Ambient operating temperature range when operating according to the diagram illustrated in Fig. 3	T_{amb}	100	°C

Characteristics of Individual Diodes at T_{amb} = 25 °C

Forward voltage at I_F = 50 mA	V_F	< 1.2	V
Reverse current at V_R = 15 V	I_R	< 500	nA
Differential forward resistance at I_F = 10 mA, f = 100 MHz	r_f	5	Ω
at I_F = 10 μA, f = 100 MHz	r_f	1.4	kΩ

Characteristics in the test circuit Fig. 3 at T_{amb} = 25 °C

Voltage for 1 % cross modulation	V_{cr}	1	V
Attenuation in the 40 . . . 1000 MHz range			
at V_{co} = 1.5 V (1 . . . 2 V)	α_{max}	45 (> 36)	dB
at V_{co} = 5 V (4 . . . 5 V)	α_{min}	1.5 (< 2)	dB
Reflection attenuation in the 40 . . . 1000 MHz range over the entire control range, depending on circuit design	α_{refl}	20 (> 16)	dB

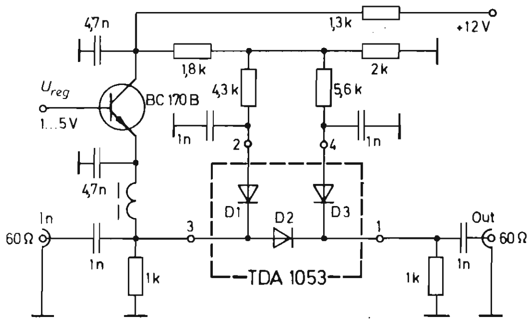


Fig. 3: Test and application circuit for the TDA 1053

Line Circuits for TV Receivers

Monolithic integrated circuits for pulse separation and line synchronization in TV receivers. Both types are identical except the output stages and the shape of their output signals. The TDA 9400 shows a Darlington emitter follower output stage (see Fig. 1), the output signal of which is suitable for driving thyristor line output stages. The output stage of the TDA 9500 (see Fig. 3) supplies signals qualified for driving transistor line output stages.

Being advanced versions of the well-known types TBA 940 and TBA 950, the new types TDA 9400 and TDA 9500 comprise the sync separator with internal noise suppression, the frame pulse integrator, the phase comparator, a switching stage for automatic changeover of noise immunity and change of the slope of the phase control circuit, the line oscillator with frequency range limiter, a highgain phase control circuit, a stage for generating the burst gate pulses in colour TV receivers, an undervoltage protection circuit and – as mentioned above – different output stages.

Due to the large scale of integration only few external components are needed. These ICs deliver prepared frame sync pulses for triggering the frame oscillator (e. g. The TDA 1044 manufactured by INTERMETALL). Their phase comparator may be switched for video recording operation. A terminal (pin 14) for phase correction with the aid of the frame parabola is provided.

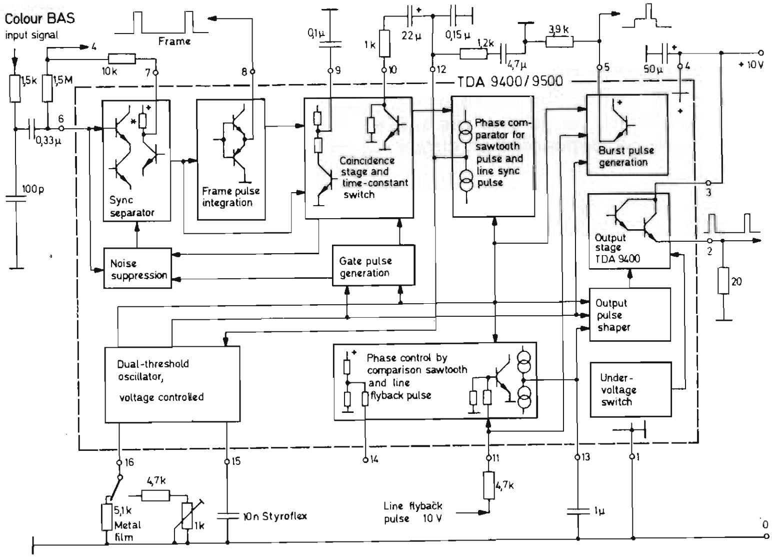


Fig. 1: Block diagram of TDA 9400/9500 and test circuit for the characteristics

* TDA 9400 has no internal pull-up resistor at pin 7

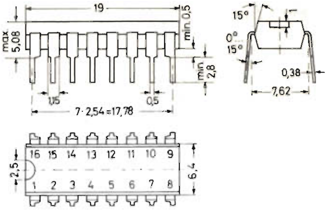


Fig. 2:
TDA 9400 and TDA 9500 in dual in-line plastic package 20 A 16 according to DIN 41 866

Weight approximately 1.2 g
Dimensions in mm

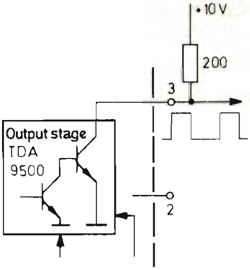


Fig. 3:
Output stage of the TDA 9500

All voltages are referred to pin 1.

Maximum Ratings

Supply voltage	V_4	14	V
Input voltage	V_6	– 6	V
Output voltages	V_3	20	V
TDA 9400 only	V_2	14	V
Output currents	I_5	– 20	mA
	$\pm I_8$	20	mA
TDA 9400	I_2	– 600	mA
TDA 9500	I_3	50	mA
Input currents	I_{11}	5	mA
	I_9	5	mA
Ambient operating temperature	T_{amb}	60	°C
Storage temperature range	T_S	–25 . . . +100	°C

Recommended Operating Conditions

Supply voltage	V_4	8 . . . 12	V
Input current during sync pulse	I_6	5 . . . 100	µA
Input signal (colour video signal)	V_{Cpp}	3 (1 . . . 6)	V
Input switching current for internal noise suppression	I_{6s}	> 0.5	mA
Input current during line flyback pulse	I_{11}	0.1 . . . 2	mA
Switching current for recording operation	I_9	> 2	mA
Input current (e. g. for frame parabola)	I_{14}	– 50 . . . +50	µA
Ambient operating temperature range	T_{amb}	0 . . . 60	°C

Characteristics at $V_3 = 10$ V, $f_o = 15\,625$ Hz, $T_{amb} = 25\,°C$, in the test circuit Fig. 1 and Fig. 3

Pin 7			
Voltage amplitude of sync signal	V_7	> 9	V
Output resistance (High-state) (only TDA 9400)	R_{A7}	2.5 (1.8 . . . 3.3)	kΩ
Pin 8			
Voltage amplitude of frame sync pulses at $\pm I_8 = 2$ mA	V_8	> 7	V
Output resistance (High-state)	R_{A8}	< 100	Ω
Frame pulse duration	t_8	150 . . . 350	µs
Delay between leading edge of frame sync pulses at pin 6 and output signal at pin 8	t_{V8}	11	µs
Pins 2 and 3			
Saturation voltage of the output transistor			
TDA 9400 at $V_3 = 10$ V, $-I_2 = 600$ mA	$V_{3/2}$	< 2.5	V
TDA 9500 in the circuit of Fig. 3	$V_{3/1}$	< 0.5	V
Output pulse duration (see Fig. 4)			
TDA 9400	t_2	4 . . . 8	µs
TDA 9500	t_3	22 . . . 30 [1]	µs
Pin 5			
Voltage amplitude of burst gate pulse at $V_4 = 12$ V (see Fig. 4)	V_{5B}	10	V
Phase shift between centre of sync pulse and leading edge of burst gate pulse	t_{B1}	1.95 ± 0.95	µs
Phase shift between centre of sync pulse and trailing edge of burst gate pulse	t_{B2}	6.75 ± 0.95	µs
Voltage amplitude of line blanking pulses at $V_4 = 12$ V (see Fig. 4)	V_{5Z}	3	V
Oscillator frequency at $C_{16/1} = 10$ nF, $R_{15/1} = 5.1$ kΩ	f_o	$15\,625 \pm 800$	Hz
Frequency pull-in and holding range	$\pm \Delta f$	650 . . . 1200	Hz
Gain of phase control loop	$\Delta t_S / \Delta t_{SR}$	> 100	
Slope of the phase comparator control loop	$\Delta f / \Delta t$	2	$\frac{\text{kHz}}{\mu\text{s}}$
Phase shift between sync pulse of the colour BAS signal and line flyback pulse at a delay $t_S = 5$ µs between leading edge of the output pulse and line flyback pulse	t_{SR}	2.6 ± 0.5	µs

[1]) delivered in groups

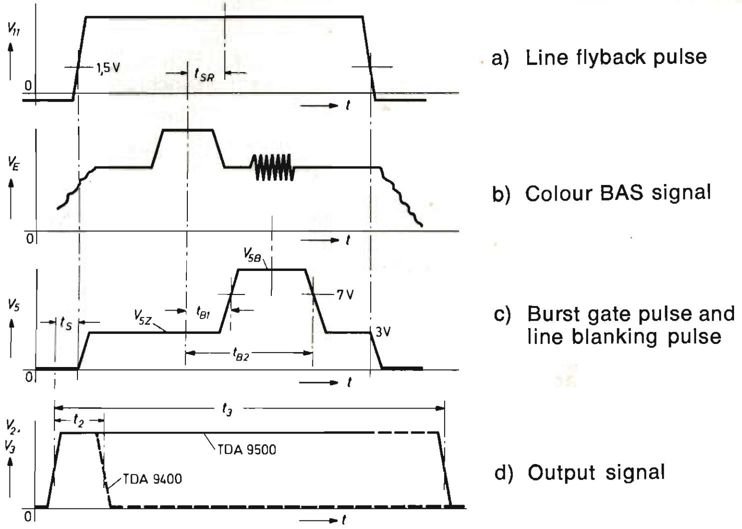


Fig. 4: Phase relations of the TDA 9400 and TDA 9500

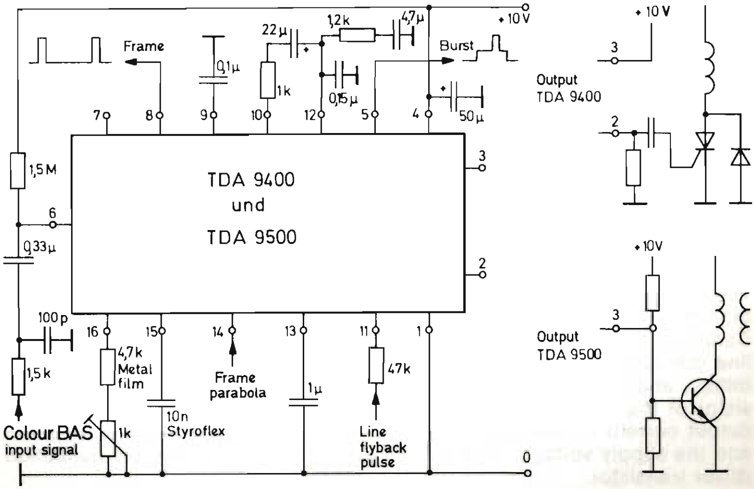


Fig. 5: Operating circuit of the TDA 9400 and TDA 9500

Design and Operation Mode of TDA 9400 and TDA 9500

The sync separator separates the synchronizing pulse from the composite colour video BAS signal. The noise inverter circuit, which needs no external components, and an internal gate-circuit free the synchronizing signal from distortion.

The frame sync pulse is obtained by internal integration and limitation of the synchronizing signal, and is available at pin 8.

The frequency of the line oscillator is determined by a 10 nF Styroflex capacitor at pin 15 which is charged and discharged periodically by two internal current sources. The external resistor at pin 16 defines the charging current and consequently in conjunction with the oscillator capacitor the line frequency.

The phase comparator compares the sawtooth voltage of the oscillator with the line sync pulse. Simultaneously an AFC voltage is generated which influences the oscillator frequency. A frequency range limiter restricts the frequency holding range.

The oscillator sawtooth voltage, which is in a fixed ratio to the line sync pulses, is compared with the line flyback pulse in the phase control circuit, in this way compensating all drift of delay times in driver and line output stage. The normal phase position is obtained if pin 14 is left vacant. Any phase displacement can be corrected by a current or voltage fed into pin 14. The duration of the output pulse is thereby not influenced.

The burst gate pulse is derived from the sawtooth voltage of the line oscillator and therefore via the phase comparator synchronized with the line sync pulses of the colour video signal.

The switching stage has different functions. When the two signals supplied by the sync separator and the phase control circuit respectively are in synchronism a saturated transistor is in parallel with the integrated 2 kΩ resistor at pin 10. Thus the time constant of the filter network at pin 12 increases and consequently reduces the pull-in range of the phase comparator circuit for the synchronized state. This arrangement ensures disturbance-free operation. Moreover, because the internal noise suppression and the internal gate circuit in synchronized operation are effective, the noise limitation is improved.

For video recording operation the automatic switchover can be blocked by a positive current fed into pin 9, e. g. via a resistor connected to pin 3. This reduces the time constant at pin 12 and increases the control current of the phase comparator thus steepening the static slope of the phase comparator which gives optimized matching in video recording operation.

The two types TDA 9400 and TDA 9500 have different output stages and different output pulse shapers. The output stage of the TDA 9400 is a Darlington emitter follower. This stage is suitable for directly driving the line deflection thyristor whereby an output current up to 600 mA is permitted, and the output stage is short-circuit protected. The output transistor of the TDA 9500 is operated in common emitter configuration. Its output current is limited to 50 mA by the pull-up resistor between pin 3 and the supply voltage. This current serves for driving the line deflection driver transistor.

If the supply voltage goes down (e. g. by switching off the mains) a built-in

protection circuit ensures defined line frequency pulses down to $V_4 = 4$ V and shuts off when V_4 falls below 4 V, thus preventing pulses of undefined duration and frequency. Conversely, if the supply voltage rises, pulses defined in duration and frequency will appear at the output pin as soon as V_4 reaches 4.5 V. In the range between $V_4 = 4.5$ V and full supply voltage the shape and frequency of the output pulses are practically constant.

ICs for Electronic Clocks

CMOS circuit for RF Quartz Clocks with Digital Adjustment and 0,5 Hz Output

The monolithic integrated CMOS circuit SAJ 300 R is intended for use in crystal-controlled clocks operating on 12 V (6 . . . 16.5 V) supply voltage.

It comprises an oscillator circuit, a fixed 4 : 1 frequency divider, a variable 21 stage divider with an adjustment range of $2^{21}:1$ to $(2^{21}+2^{9}):1$ and a motor driver stage. An integrated Zener diode with approximately 17 V operating voltage protects the IC against voltage peaks on the supply voltage.

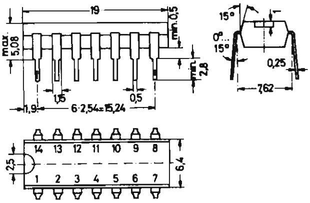
Apart from the crystal the oscillator requires no additional components. The trimmer capacitor previously needed for frequency adjustment has been omitted and this simplifies the layout of the clock. The function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose, seven adjustment terminals are provided on the SAJ 300 R: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. With an oscillator frequency of 4.194812 MHz, the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 0.5 Hz if the variable frequency divider is set to the centre. Due to the differentiating effect of the motor capacitor pulses of alternate direction and one second distance originate in the motor coil.

The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 14. If one or more adjustment terminals are grounded (taken to pin 13), the output frequency decreases. Pin 7 gives the smallest adjustment of 1.9 ppm. Pin 6 affords the next-larger step of 3.8 ppm and so forth, up to pin 1 which enables an adjustment step of 122 ppm to be obtained. Thus, if all adjustment terminals are grounded, the output frequency is reduced by 242 ppm.

The by-four-divided oscillator frequency may be checked at a separate test terminal M (pin 8) non-reactive with respect to the oscillator. Based on this check the output frequency and consequently the accuracy of the clock may be adjusted at the terminals 1 . . . 7 by means of the variable frequency divider.

Fig. 1:
SAJ 300 R in dual in-line (Dil) plastic TO-116 package
24 A 14 according to DIN 41 866

Weight approximately 1.1 g
Dimensions in mm



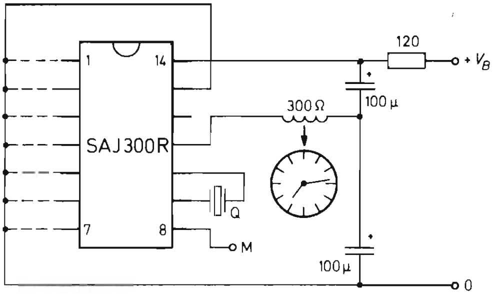


Fig. 2: Operating circuit of the SAJ 300 R in a quartz controlled clock

All voltages are referred to pin 13.

Maximum Ratings

Supply voltage	V_B	– 0.3 . . . + 18	V
Output current	$\lvert I_{11} \rvert$	60	mA
Current load of the test output	$\lvert I_8 \rvert$	0.1	mA
Power dissipation at T_{amb} = 25°C	P_{tot}	300	mW
Ambient operating temperature range	T_{amb}	– 45 . . . + 85	°C
Storage temperature range	T_S	– 55 . . . + 125	°C

Recommended Operating Conditions

Supply voltage	V_{14}	6 . . . 16.5	V
Parallel resonance frequency of the quartz at C_L = 16 pF	f_p	4.194812	MHz
Effective series resistance of the quartz at C_L = 16 pF	R'_r	< 150	Ω
Output load resistance	R_L	> 250	Ω

Characteristics at V_{14} = 12 V , Quartz 4.194812 MHz, T_{amb} = 25 °C

Current consumption at open output	I_{14}	3	mA
Output frequency at centre position of the variable divider	f_o	0.5	Hz
Frequency at test output	f_M	1.048703	MHz
Range of output frequency adjustment	$\Delta f_o/f_o$	± 121	ppm
Accuracy of output frequency adjustment	df_o/f_o	± 0.95	ppm
Output pulse duration	t_o	1	s
Output resistance at V_{14} = 6 V	r_o	100	Ω

CMOS Circuit for RF Quartz Clocks with Digital Adjustment and 64 Hz Output

The monolithic integrated CMOS circuit SAJ 300 T is intended for use in crystal-controlled clocks operating on 12 V (6 . . . 16.5 V) supply voltage. It comprises an oscillator circuit, a fixed 4 :1 frequency divider, an adjustable frequency divider and a motor driver stage. The adjustable frequency divider may be adjusted in 127 steps, covering the range from $2^{14}:1$ to $(2^{14}+2^{2}):1$.

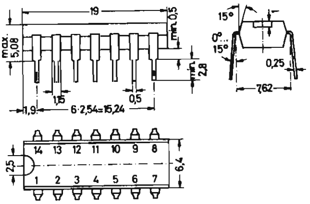
Apart from the crystal the oscillator requires no additional components. The trimmer capacitor previously needed for frequency adjustment has been omitted and this simplifies the layout of the clock. The function of the trimmer capacitor has been taken over by the variable frequency divider comprised in the IC and used to set the correct output frequency. For this purpose seven adjustment terminals are provided on the SAJ 300 T: they are used to set the divider ratio to the required value with an accuracy of 10^{-6}. With an oscillator frequency of 4.194 812 MHz, the series-connected push-pull output stage supplies a symmetrical square wave signal with a pulse duty factor of 0.5 and a repetition frequency of 64 Hz if the variable frequency divider is set to the centre. Due to the differentiating effect of the motor capacitors pulses of alternate direction and 7.8 ms distance originate in the motor coil.

The adjustable frequency divider has been designed in such a way that the maximum output frequency is set when all adjustment terminals are either open-circuit or connected to pin 14. If one or more adjustment terminals are grounded (taken to pin 13), the output frequency decreases. Pin 7 gives the smallest adjustment of 1.9 ppm. Pin 6 offers the nextlarger step of 3.8 ppm and so forth, up to pin 1 which enables an adjustment step of 122 ppm to be obtained. Thus, if all adjustment terminals are grounded, the output frequency is reduced by 242 ppm.

The by-four-divided oscillator frequency may be checked at a separate test terminal M (pin 8) non-reactive with respect to the oscillator. Based on this check the output frequency and consequently the accuracy of the clock may be adjusted at the terminals 1 . . . 7 by means of the variable frequency divider.

Fig. 1:
SAJ 300 T in dual in-line (Dil) plastic TO-116 package
20 A 14 according to DIN 41 866

Weight approximately 1.1 g
Dimensions in mm



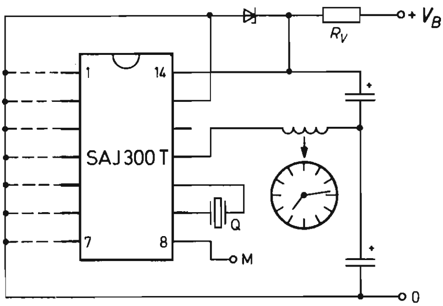


Fig. 2: Operating circuit of the SAJ 300 T in a quartz-controlled clock

All voltages are referred to pin 13.

Maximum Ratings

Supply voltage	V_{14}	–0.3 . . . +18	V
Output current	$\|I_{11}\|$	60	mA
Current load of the test output	$\|I_8\|$	0.1	mA
Power dissipation at T_{amb} = 25 °C	P_{tot}	300	mW
Ambient operating temperature range	T_{amb}	–45 . . . +85	°C
Storage temperature range	T_S	–55 . . . +125	°C

Recommended Operating Conditions

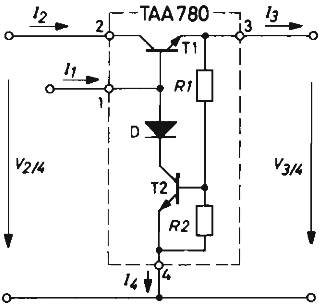
Supply voltage	V_{14}	6 . . . 16.5	MHz
Parallel resonance frequency of the quartz at C_L = 16 pF	f_p	4.194 812	MHz
Effective series resistance of the quartz at C_L = 16 pF	R'_r	< 150	Ω
Output load resistance	R_L	> 250	Ω

Characteristics at V_{14} = 12 V, Quartz 4.194 812 MHz, T_{amb} = 25 °C

Current consumption (open output)	I_{14}	3	mA
Frequency at test output pin 8	f_M	1.048 703	MHz
Output frequency at centre position of the variable divider	f_o	64	Hz
Range of output frequency adjustment	$\Delta f_o/f_o$	±121	ppm
Accuracy of output frequency adjustment	df_o/f_o	±0.95	ppm
Output pulse duration	t_o	7.8	ms
Output resistance at V_{14} = 6 V, R_L = 300 Ω	r_o	100	Ω

1.1 V Stabilizing Circuit

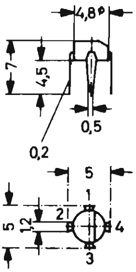
Monolithic integrated circuit, e. g. for the voltage-stabilized drive of clocks and for the stabilization of the operating point in transistor circuits. The circuit comprises the operating transistor T1 (see fig. 1) and a control circuit for the stabilization of the output voltage $V_{3/4}$ to 1.1 V.



T1:	Operating transistor
T2:	Regulation transistor
D:	Blocking diode
R1, R2:	Voltage divider

Fig. 1: Internal circuitry and test circuit

Fig. 2:
TAA 780 in plastic package
50 B 4 according to DIN 41 867
Weight approx. 0.1 g
Dimensions in mm



All characteristics and maximum ratings indicated below refer to the test circuit (Fig. 1). The figure 0 in the index of some characteristics means that in this case all other pins are open.

The following definitions apply:

$$S_{V3/4} = \frac{\Delta V_{2/4} \cdot V_{3/4}}{\Delta V_{3/4} \cdot V_{2/4}} \quad \text{and} \quad \alpha_{V3/4} = \frac{\Delta V_{3/4}}{V_{3/4} \cdot \Delta T_{amb}}$$

Maximum Ratings

Collector base voltage	$V_{2/1/0}$	3	V
Collector emitter voltage for $R_{1/3} = 5\ k\Omega$ (ext. connected)	$V_{2/3R}$	2	V
Emitter base voltage	$V_{3/1/0}$	2	V
Substrate base voltage	$V_{4/1/0}$	2	V
Collector current	I_2	15	mA
Stabilizing current	I_1	1	mA
Ambient temperature range	T_{amb}	−20 ... +40	°C
Storage temperature range	T_S	−20 ... +125	°C

Characteristics at $T_{amb} = 25\ °C$

DC current gain of transistor T1 at $V_{2/3} = 1.5\ V$, $I_2 = 0.3\ mA$, $I_4 = 0$	$B_{0.3}$	250 (> 120)	
Collector saturation voltage of transistor T1 at $I_2 = 3.5\ mA$, $I_1 = 35\ \mu A$, $I_4 = 0$	$V_{2/3\ sat}$	0.1 (< 0.12)	V
Base saturation voltage of transistor T1 at $I_2 = 3.5\ mA$, $I_1 = 35\ \mu A$, $I_4 = 0$	$V_{1/3\ sat}$	0.7	V
Total resistance of voltage divider	$R1 + R2$	15 (> 10)	kΩ
Stabilized voltage at $V_{2/4} = 1.5\ V$, $I_1 = 250\ \mu A$, $I_3 = 3.5\ mA$	$V_{3/4}$	1.1 ± 0.06	V
Voltage stabilization coefficient at $V_{2/4} = 1.3 \ldots 1.7\ V$, $I_1 = 250\ \mu A$, $I_3 = 3.5\ mA$	$S_{V3/4}$	−200	
Temperature coefficient of the stabilized voltage at $V_{2/4} = 1.5\ V$, $I_1 = 250\ \mu A$, $I_3 = 3.5\ mA$	$\alpha_{V3/4}$	$-2.8 \cdot 10^{-3}$	1/°C
Small signal current gain of transistor T1 at $V_{2/3} = 1.5\ V$, $I_2 = 0.3\ mA$, $I_4 = 0$	h_{fe}	250	

Fig. 3:
Variation of output voltage $V_{3/4}$ with input voltage $V_{2/4}$, referred to $V_{2/4}=1.5\,V$, $V_{3/4}=1.1\,V$

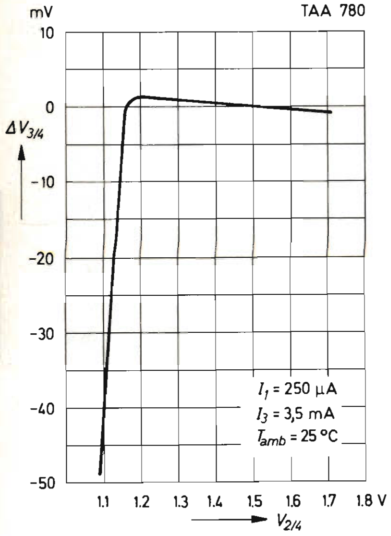


Fig. 4:
Variation of output voltage $V_{3/4}$ with current I_1 referred to $I_1=250\,\mu A$, $V_{3/4}=1.1\,V$

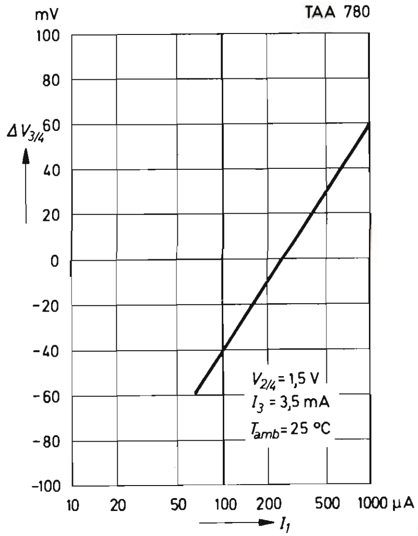
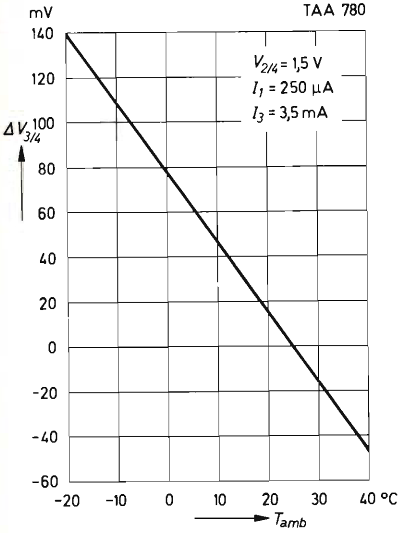


Fig. 5:
Variation of output voltage $V_{3/4}$ with ambient temperature referred to $T_{amb}=25\,°C$, $V_{3/4}=1.1\,V$



Driving Circuit for Clocks with Single-Coil Balance Systems

This monolithic integrated circuit in bipolar technique is intended for driving clocks (wall and table models) with single-magnet, single-coil balance systems.

The TCA 860 simplifies the design of the clock circuitry and stabilizes the balance wheel amplitude against external mechanical influences as well as against supply voltage changes.

The circuit is operated from a conventional battery. Its current consumption is low.

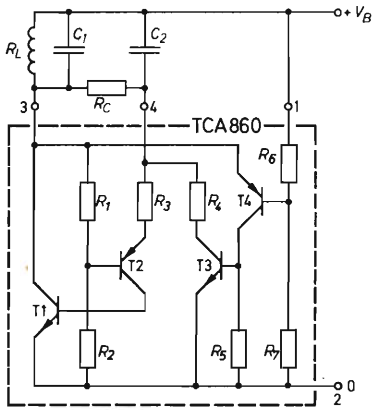
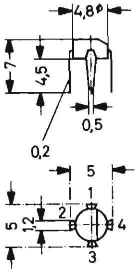


Fig. 1: Internal circuitry and operating circuit

Fig. 2: TCA 860 in plastic package 50 B 4 according to DIN 41 867

Weight approximately 0.1 g
Dimensions in mm



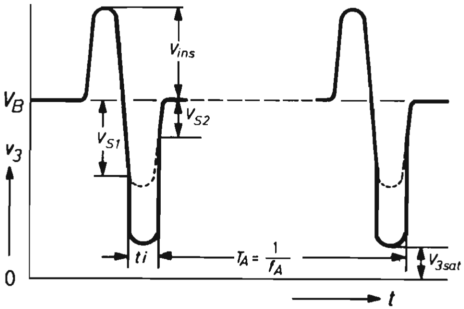


Fig. 3: Voltage v_3 as a function of time in a single-magnet balance system

All voltages are referred to pin 2.

Maximum Ratings

Supply voltage	V_B	3	V
Currents	I_1, I_3, I_4	10	mA
Ambient operating temperature range	T_{amb}	− 10 . . . + 60	°C

Recommended Operating Conditions

Supply voltage	V_B	1.5 (1.1 . . . 1.65)	V
Frequency of driving pulses	f_A	5 (2 . . . 8)	Hz
Capacitor	C_1	0.22 (0.1 . . . 0.33)	µF
	C_2	15 (10 . . . 22)	µF
Induced voltage at nominal amplitude	$V_{in\,s}$	550	mV
Coil resistance	R_L	250 (200 . . . 300)	Ω
Discharge resistor	R_C	180	kΩ

Test Conditions for the Characteristics

The characteristics of the TCA 860 are tested by a method which is independent of the properties of a particular clock mechanism. For this reason, the multivibrator properties of the TCA 860 are utilised in the test circuit as shown in Fig. 4. The pulse frequency of the circuit (Fig. 5) is inversely proportional to the value of capacitor C_2. It should be chosen so that automatic test equipment may be used.

Operation as Multivibrator

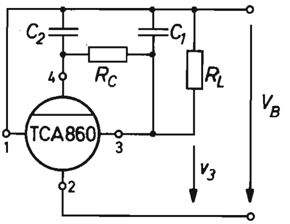


Fig. 4: Test circuit

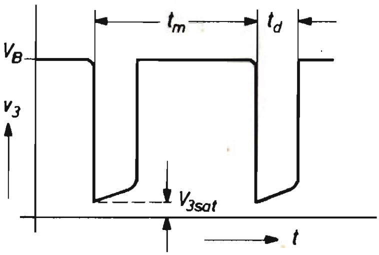


Fig. 5: Shape of voltage v_3

Characteristics at $V_B = 1{,}5$ V, $R_L = 330\ \Omega$, $R_C = 180$ kΩ
$C_1 = 0{,}1\ \mu$F, $C_2 = 1\ \mu$F, $T_{amb} = 25\ ^\circ$C

Duration of period	t_m	40 . . . 90	ms
Pulse duration	t_d	4,5 . . . 16	ms
Saturation voltage	V_{3sat}	$<$ 250	mV

Hints for the Design of Circuits with TCA 860

The optimum conditions for the driving pulse exist when it ends before the induced voltage approaches zero. This condition depends on the choice of capacitance C_2, the discharge resistance R_C, and the properties of the movement such as induced voltage $V_{in\ s}$, driving frequency f_A, pulse duty factor t_i/T_A and coil resistance R_L.

The value of capacitance C_1 must be large enough to cut the voltage peaks caused by the coil inductance at steady state operation to a level less than the maximum value of the coil voltage v_3 (Fig. 3).

In order to ensure optimum amplitude control of the TCA 860 the positive voltage pulse must occur before the negative pulse as shown in Fig. 3.

The self-starting properties of an oscillating system depend mainly upon the characteristics of the balance system and the coil. The starting time is determined by the moment of inertia of the balance wheel, the magnet system, the value of the induced coil voltage and the coil resistance.

Fig. 6:
Balance wheel amplitude versus supply voltage

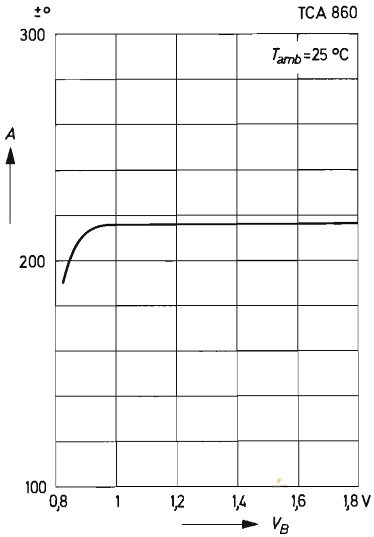
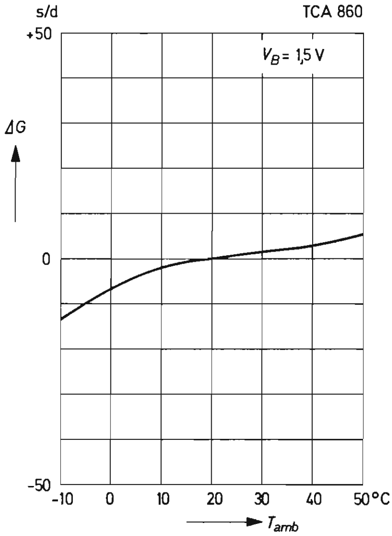


Fig. 7:
Accuracy versus ambient temperature



These two curves were derived from measurements on a typical clock.

ICs for Motor Vehicles

Pulse Shaper for Revolution Counters

The monolithic integrated circuit SAK 215 is designed for use in revolution counters of cars and for other applications like frequency to current converters. By use of suitable external circuitry the revolution counter can be adapted to engines with two to eight cylinders. It is designed for a nominal 12 V DC supply.

Fig. 1 shows the operating circuit of a revolution counter with FSD = 6000 RPM (two ignition pulses per turn of the crank-shaft) at a nominal battery voltage of 12 V.

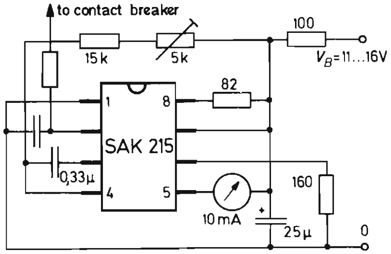
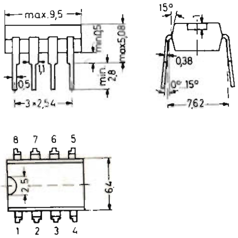


Fig. 1: Block diagram and operating circuit of the SAK 215

Fig. 2:
SAK 215 in mini Dip
plastic package similar to TO-116

Weight approximately 0.5 g
Dimensions in mm



All voltages are referred to pin 1.

Maximum Ratings

Supply voltage	see dimensioning hints for R_V and $R_{7/8}$		
Input voltage	V_2	±20	V
Current through instrument coil	I_5, $-I_6$	40	mA
Ambient operating temperature range	T_{amb}	−25 ... +65	°C
Storage temperature range	T_S	−25 ... +125	°C
Total power dissipation at T_{amb} = 65 °C	P_{tot}	500	mW

Recommended Operating Conditions

Frequency of the input pulses	f_i	< 10	kHz
Pulse duty factor of output current	t_{p5}/T_5	< 0.9	
Timing resistor	$R_{7/4}$	15 ... 100	kΩ
Resistor for adjusting the current through the instrument coil	$R_{6/1}$	> 100	Ω
Voltage drop across by-pass resistor	$V_{7/8}$	< 7	V
Voltage drop between pins 5 and 6	$V_{5/6}$	> 1	V

Test Conditions for the Characteristics (see test circuit Fig. 3)

Supply voltage	V_B	14	V
Ambient operating temperature	T_{amb}	25	°C
Input pulse amplitude	V_2	1.6	V
Input pulse duration	t_i	0.5	ms
Input pulse repetition frequency	f_i	250	Hz

Characteristics in the test circuit Fig. 3

Supply voltage	V_7	7.4 ... 8.2	V
Current consumption	I_7	< 12	mA
Input voltage range without triggering the circuit	V_2	−20 ... +0.5	V
Trigger range	V_2	1.5 ... 20	V
Trigger slope	dV_2/dt	positive-going	
Input impedance	$r_{2/1}$	7	kΩ
Pulse amplitude at pin 6	V_6	2 ... 2.5	V
Output pulse duration	t_5	$0.64 \cdot R_{7/4} \cdot C_{3/4}$	
Output current	I_5	$-I_6$	

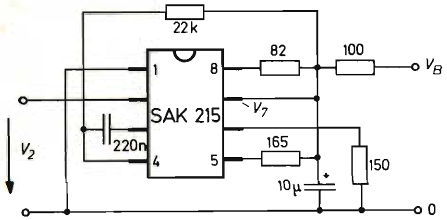


Fig. 3: Test circuit for the characteristics

Dimensioning Hints

Coil resistance R_M of the indicating instrument

The output transistor must operate in the active range. This is ensured if

$$V_{5/6} = V_7 - V_6 - (I_{5p} \cdot R_M)$$

is above 1 V. The additional inductive voltage drop at the beginning of a current pulse due to the inductance of the moving coil is ignored in this equation.

Adjustment resistor $R_{6/1}$ for the instrument current

The peak current through the moving coil is given at a pulse duty factor of 0.7 by

$$I_{5p} = \frac{I_M}{0.7}$$

where I_M is the DC current for full scale deflection. Since the current flowing into pin 5 is equal to the sink current of pin 6 the adjustment resistor $R_{6/1}$ can be calculated as

$$R_{6/1} = \frac{V_6}{I_{5p}}$$

Series resistor R_V

Between pin 7 and pin 1 the circuit behaves like a zener diode. The resistor R_V therefore has to be chosen so that adequate current for the IC and the moving coil is available even at the lowest battery voltage:

$$R_V \leq \frac{V_B\,min - 8.2\text{ V}}{12\text{ mA} + I_{5p}}$$

By-pass resistor $R_{7/8}$

In order to ensure proper function of the stabilizing circuit the voltage drop across the by-pass resistor $R_{7/8}$ must be limited to 7 V at the highest battery voltage.

$$R_{7/8} < \frac{7\text{ V} \cdot R_V}{V_{B\,max} - 7.4\text{ V}}$$

Speedometer and Mileage Indicator

The monolithic integrated circuit SAY 115 is designed for use in electronic speedometer and mileage indicator systems in automobiles.

It comprises a monostable flip-flop with Schmitt trigger input and an output stage comprising a current source whose current is indicated by a moving coil instrument (see Fig. 1). A binary frequency divider followed by a doubled output stage controls a stepping motor with two windings for mileage indication. The frequency divider of the SAY 115 X consists of five and at the SAY 115 Y of six stages. An analogue output controlled by the monostable flip-flop may be used to obtain an additional signal when an arbitrarily selected speed is exceeded or when the speed falls below the desired level.

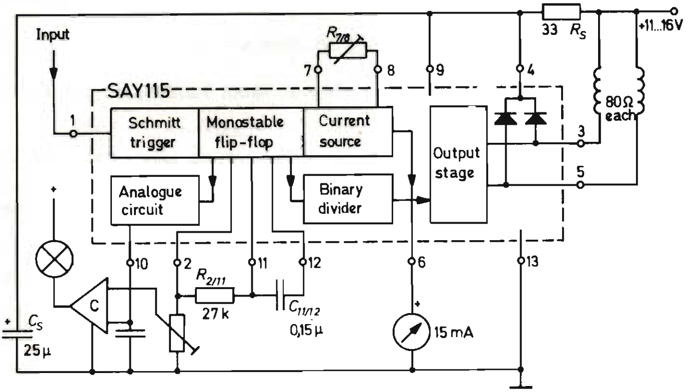
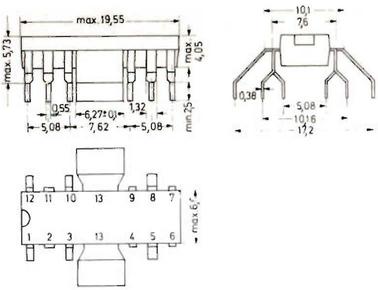


Fig. 1: Circuit of an electronic speedometer with FSD at f_i = 300 Hz

Fig. 2:
SAY 115 in dual in-line plastic package

Weight approx. 1.5 g
Dimensions in mm



The input signal for the SAY 115 is preferably derived from the gearbox via a reed contact, a make-and-break oscillator or an inductive sensor. The monostable flip-flop is triggered during the trailing edge of the input signal; a possible bouncing of the grounded reed contact can therefore not produce faulty indications, since such bouncing coincides with the metastable period of the flip-flop. The shape of the input pulses is irrelevant, provided that the predetermined upper and lower thresholds are reliably attained. The pulse duration produced by the monostable flip-flop is determined by the *RC*-network $R_{2/11}$, $C_{11/12}$. It is subject to variation within wide limits and capable of being adapted to the input frequency.

The mean output current from pin 6, which is a linear function of the input frequency, can be adjusted by using the trimmer potentiometer $R_{7/8}$. It is possible to use either $R_{7/8}$ or $R_{2/11}$ for calibrating the speedometer. Since the indicating instrument is supplied from a current source, temperature-dependent variations of the instrument coil resistance do not affect the indication. The temperature response of the indication is determined only by the components $R_{2/11}$, $R_{7/8}$ and $C_{11/12}$, since the drift of the current source is negligible. As a result, there is virtually no warm-up error that can affect the indication when the supply voltage is turned on. One terminal of the moving coil instrument is grounded which simplifies the mechanical layout.

If a filter capacitor is added to the analogue output, a DC voltage is obtained which is a linear function of speed. Using a comparator *C*, an alarm signal can be produced when the speed exceeds or falls below an arbitrarily chosen value. The reference voltage needed for the second comparator input may be derived by means of a voltage divider (trimmer potentiometer) from the stabilised 6.5 V available at pin 2. The level of the switching threshold in this arrangement depends only upon the temperature response of the comparator, the voltage divider and the *RC* network $R_{2/11}$, $C_{11/12}$.

The binary divider of the SAY 115 X consists of five stages (dividing the input frequency by $2^5 = 32$) and the divider of the SAY 115 Y consists of six stages (dividing factor $2^6 = 64$). The reduced frequency drives the double output stage, each part consisting of an NPN Darlington pair. One of the two output stages is always low and the other one high in turn of any half-period of the output signal. Each output is provided with an integrated free-running diode, whose cathodes being connected to pin 4.

In order to protect the integrated circuit against high voltage peaks from the car supply system, an external filtering network for the supply voltage must be provided. The motor supply current does not flow through the resistor of the filtering network; reliable starting of the stepping motor is thus ensured even in the case of low battery voltages. The cooling fins of the package (pin 13) form the ground pin of the SAY 115; they must be soldered to the copper layer of the printed circuit board in such a way that good heat conduction is achieved.

All voltages are referred to pin 13 (ground).

Maximum Ratings

Supply voltage, continuous	V_9	16	V
Supply voltage, duration $t < 5$ ms	V_9	20	V
Input voltage	V_1	−0.5 . . . +20	V

Maximum Ratings, continued

Output currents	I_3, I_5	300	mA
	I_6	–30	mA
Ambient operating temp. range	T_{amb}	–40 . . . +80	°C
Storage temperature range	T_S	–40 . . . +125	°C

Recommended Operating Conditions

Supply voltage	V_B	11 . . . 16	V
Input frequency	f_{in}	< 10	kHz
Timing resistor	$R_{2/11}$	15 . . . 100	kΩ
Pre-set resistor for current source	$R_{7/8}$	> 100	Ω
Pulse duty factor of the monostable	t_{p6}/T_6	< 0.9	
Filter resistor	R_S	33	Ω
Filter capacitor	C_S	> 25	µF

Characteristics for $V_9 = 11 \ldots 16$ V, $T_{amb} = 25$ °C

Quiescent current consumption without motor	I_9	16	mA
Input trigger thresholds	V_{IL}	2.5	V
	V_{IH}	3.5	V
Input current at $V_I < V_{IL}$	I_I	–100	µA
at $V_I > V_{IH}$	I_I	0	

Triggering of the monostable flip-flop is effected by the trailing edge of the input signal when it falls below V_{IL}.

Reference voltage	V_2	6.5	V
Current source operating range at pin 6	V_6	0 . . . 5	V
Peak current through the moving coil instrument	I_{6p}	$\frac{2.3\text{ V}}{R_{7/8}}$	
Output pulse duration pin 6	t_{p6}	$0.67 \cdot R_{2/11} \cdot C_{11/12}$	
DC voltage at the analogue output for $f = 0$	V_{10}	6.5	V
for $f = f_{max}$ (pulse duty factor $t_{p6}/T_6 = 0.9$)	V_{10}	2.1	V
Output resistance of the analogue output	$R_{out\,10}$	10	kΩ

Divider ratio of the binary divider			
SAY 115 X	f_i/f_o	32	
SAY 115 Y	f_i/f_o	64	
Saturation voltage at the motor output pins at I_3 and I_5 = 200 mA	V_{sat}	1.2	V

Car Voltage Stabilizer

Monolithic integrated voltage stabilizer in bipolar technology, specially designed for stabilized power supplies of car instrumentation in vehicles with 12 V accumulators.

This IC features narrow tolerance on output voltage, a low temperature coefficient and is equipped with an automatic current limiter and a thermal overload protection which prevents destruction of the IC in case of accidental overloads, for example short-circuits. A sufficiently large cooling fin must be provided, to ensure that under normal working conditions the max. permissible junction temperature is not exceeded, and the thermal overload protection does not operate.

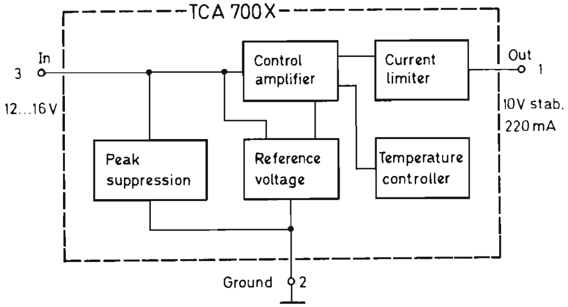
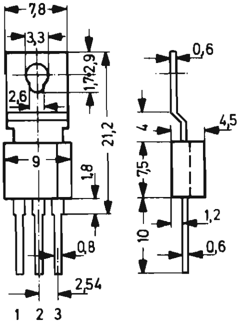


Fig. 1: Block diagram

Fig. 2:
TCA 700 X in plastic case similar to 34 A 3
Pin 2 (ground) is connected to the cooling fin.

Weight approximately 1.5 g
Dimensions in mm



All voltages are referred to pin 2.

Maximum Ratings

Input voltage continuously	V_3	−0.5 ... +16	V
pulsed, max. 1 s	V_3	20	V
pulsed, max. 0.1 ms with R_i = 100 Ω	V_3	200	V
Input current, pulsed, decaying according to an e-function with $\tau = 1$ ms	$-I_3$	15	A
Junction temperature	T_j	125	°C
Storage temperature range	T_S	−40 ... +125	°C

Recommended Operating Conditions

Load resistance	$R_{1/2}$	> 45.5	Ω

Characteristics at R_{thS} = 20 °C/W [1]), T_{amb} = 25 °C

Stabilized voltage at V_3 = 12 ... 16 V, $R_{1/2}$ = 45.5 ... 330 Ω	V_1	9.775 ... 10.225	V
at V_3 = 11.5 V, $R_{1/2}$ = 45.5 Ω	V_1	> 9.65	V
at V_3 = 10.8 V, $R_{1/2}$ = 45.5 Ω	V_1	> 8.95	V
Temperature dependence of the stabilized voltage at V_3 = 13.5 V, $R_{1/2}$ = 70 Ω	$\frac{\Delta V_1}{\Delta T_C}$	+1	mV/°C
Current limiting starts at	$-I_1$	> 220	mA
Current consumption at $I_1 = 0$	I_3	8	mA
Thermal resistance junction to contact surface	R_{thC}	< 10	°C/W

[1]) R_{thS} is the thermal resistance between cooling fin and ambient air.

ICs for Electronic Organs

Seven Stage Frequency Divider in I²L Technique

triggerable by the positive flank of the input signal

Monolithic integrated circuit in I²L technique designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs. It is pin compatible with the SAJ 110 seven stage frequency divider.

The individual flip-flops can be interconnected to form a divider chain. Some flip-flop stages are already internally series-connected as shown below. The SAA 1004-N may be driven by sinusoidal as well as by squarewave input signals. The flip-flops change state with each positive-going flank of the input voltage (see Fig. 3).

Special features are: low impedance push-pull outputs, high input impedance, low current consumption and wide supply voltage operating range.

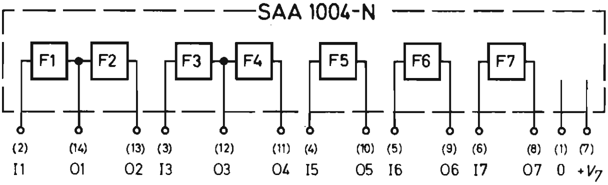
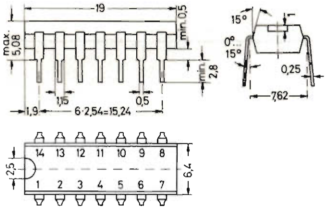


Fig. 1: Block diagram of the SAA 1004-N
The figures in brackets correspond to the pin numbers

Fig. 2:
SAA 1004-N in plastic package 20 A 14 according to DIN 41 866

Weight approximately 1.1 g
Dimensions in mm



All voltages are referred to pin 1.

Maximum Ratings

Supply voltage	V_7	15.5	V
Input voltage	V_I	$\leq V_7$	
Output current per stage	I_O	± 5	mA
Ambient operating temperature range	T_{amb}	$-10 \ldots +60$	°C
Storage temperature range	T_S	$-30 \ldots +125$	°C

Characteristics per Divider Stage at $V_7 = 9$ V, $R_L = 5.6$ kΩ, $T_{amb} = 25$ °C

Current consumption (unloaded)	I_7	0.8	mA
Input threshold voltage (see Fig. 4)	V_{IH}	6	V
	V_{IL}	2	V
Input resistance	r_i	40	kΩ
Output voltage high state R_L connected to pin 1	V_{OH}	$V_7 - 0.9$ V	
Output voltage low state R_L connected to pin 7	V_{OL}	0.3	V
Output resistance high state	r_H	100	Ω
Output resistance low state	r_L	200	Ω
Rise time of the output voltage	t_r	100	ns
Fall time of the output voltage	t_f	100	ns

Recommended Operating Conditions

Supply voltage	V_7	$7 \ldots 15$	V
Input trigger voltage	V_{IH}	$> (V_7 - 1$ V)	
	V_{IL}	< 1	V
Load resistance at the output (connected to pin 1 or pin 7)	R_L	> 5.6	kΩ
Maximum input frequency	f_{max}	50	kHz

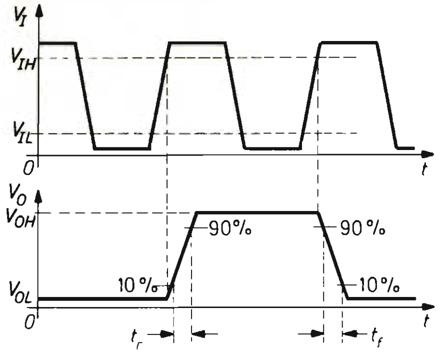


Fig. 3: Pulse diagram of a divider stage

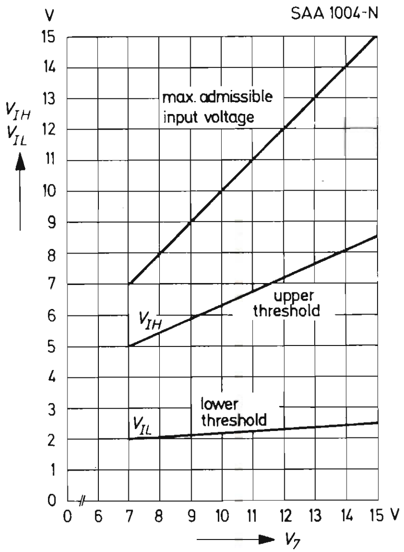


Fig. 4: Typical trigger range and admissible input voltage versus supply voltage

Seven Stage Frequency Divider in I²L Technique
triggerable by the negative flank of the input signal

Monolithic integrated circuit in I²L technique designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs. It is pin compatible with many MOS frequency dividers used in electronic organs.

The individual flip-flops can be interconnected to form a divider chain. Some flip-flop stages are already internally series-connected as shown below. The SAA 1005 may be driven by sinusoidal as well as by square-wave signals. The flip-flops change state with each negative-going flank of the input voltage (see Fig. 3).

Special features are: low-impedance push-pull outputs, high input impedance, low current consumption and wide supply voltage operating range.

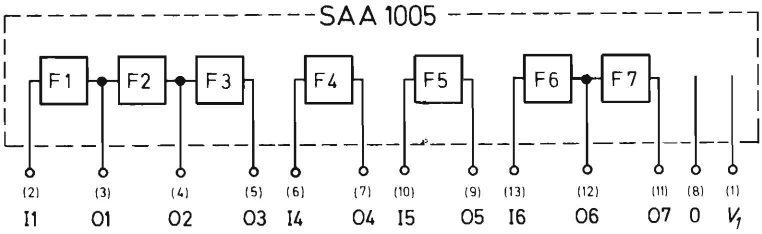
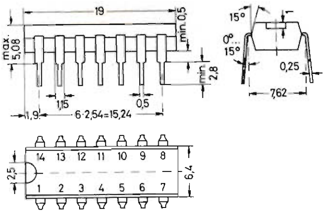


Fig. 1: Block diagram of the SAA 1005
The figures in brackets correspond to the pin numbers

Fig. 2:
SAA 1005 in plastic package
20 A 14 according to DIN 41 866

Weight approximately 1.1 g
Dimensions in mm



All voltages are referred to pin 8.

Maximum Ratings

Supply voltage	V_1	15.5	V
Input voltage	V_I	V_1	
Output current per stage	I_O	± 5	mA
Ambient operating temperature range	T_{amb}	– 10 . . . +60	°C
Storage temperature range	T_S	– 30 . . . +125	°C

Characteristics per Divider Stage at $V_1 = 12$ V, $R_L = 10$ kΩ, $T_{amb} = 25$ °C

Current consumption (unloaded)	I_1	0.8	mA
Input threshold voltage (see Fig. 4)	V_{IH}	7	V
	V_{IL}	2.5	V
Input resistance	r_i	40	kΩ
Output voltage high state R_L connected to pin 8	V_{OH}	$V_1 - 0.9$ V	
Output voltage low state R_L connected to pin 1	V_{OL}	0.3	V
Output resistance high state	r_H	100	Ω
Output resistance low state	r_L	200	Ω
Rise time of the output voltage	t_r	100	ns
Fall time of the output voltage	t_f	100	ns

Recommended Operating Conditions

Supply voltage	V_1	7 . . . 15	V
Input trigger voltage	V_{IH}	$> (V_1 - 1$ V)	
	V_{IL}	< 1	V
Load resistance at the output (connected to pin 1 or pin 8)	R_L	> 5.6	kΩ
Maximum input frequency	f_{max}	50	kHz

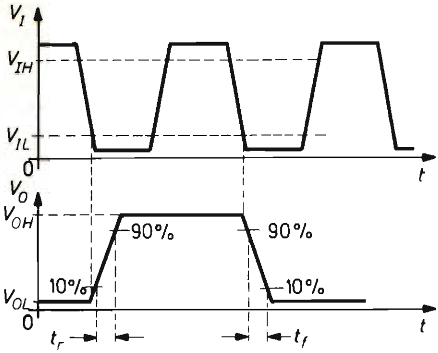


Fig. 3: Pulse diagram of a divider stage

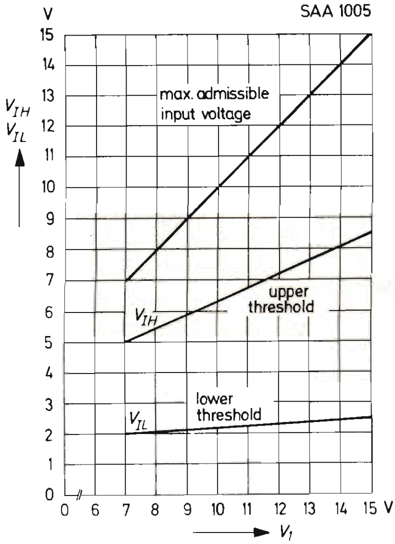


Fig. 4: Typical trigger range and admissible input voltage versus supply voltage

Seven Stage Frequency Divider in I²L Technique
triggerable by the positive flank of the input signal

Monolithic integrated circuit in I²L technique designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs. It is pin compatible with many MOS frequency dividers used in electronic organs.

The individual flip-flops can be interconnected to form a divider chain. Some flip-flop stages are already internally series-connected as shown below. The SAA 1005-P may be driven by sinusoidal as well as by square-wave signals. The flip-flops change state with each positive-going flank of the input voltage (see Fig. 3).

Special features are: low-impedance push-pull outputs, high input impedance, low current consumption and wide supply voltage operating range.

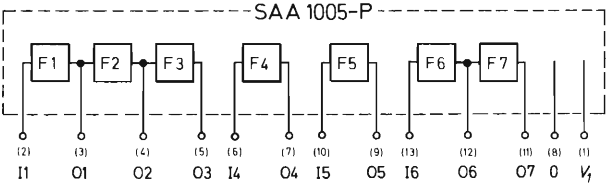
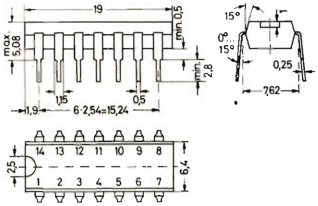


Fig. 1: Block diagram of the SAA 1005-P
The figures in brackets correspond to the pin numbers

Fig. 2:
SAA 1005-P in plastic package
20 A 14 according to DIN 41 866

Weight approximately 1.1 g
Dimensions in mm



All voltages are referred to pin 8.

Maximum Ratings

Supply voltage	V_1	15.5	V
Input voltage	V_I	V_1	
Output current per stage	I_O	± 5	mA
Ambient operating temperature range	T_{amb}	– 10 . . . +60	°C
Storage temperature range	T_S	– 30 . . . +125	°C

Characteristics per Divider Stage at $V_1 = 12$ V, $R_L = 10$ kΩ, $T_{amb} = 25$ °C

Current consumption (unloaded)	I_1	0.8	mA
Input threshold voltage (see Fig. 4)	V_{IH}	7	V
	V_{IL}	2.5	V
Input resistance	r_i	40	kΩ
Output voltage high state R_L connected to pin 8	V_{OH}	V_1 – 0.9 V	
Output voltage low state R_L connected to pin 1	V_{OL}	0.3	V
Output resistance high state	r_H	100	Ω
Output resistance low state	r_L	200	Ω
Rise time of the output voltage	t_r	100	ns
Fall time of the output voltage	t_f	100	ns

Recommended Operating Conditions

Supply voltage	V_1	7 . . . 15	V
Input trigger voltage	V_{IH}	$> (V_1 - 1$ V)	
	V_{IL}	< 1	V
Load resistance at the output (connected to pin 1 or pin 8)	R_L	> 5.6	kΩ
Maximum input frequency	f_{max}	50	kHz

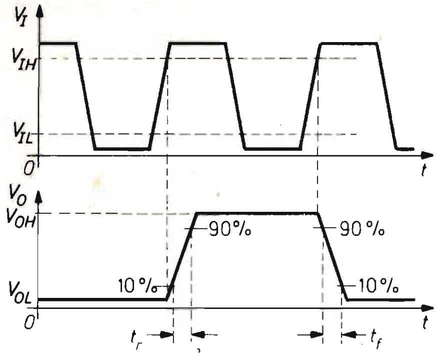


Fig. 3: Pulse diagram of a divider stage

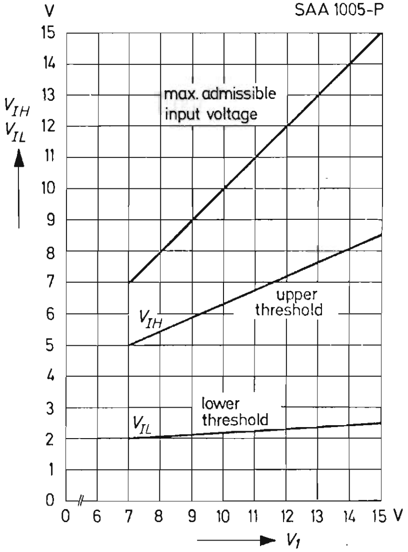


Fig. 4: Typical trigger range and admissible input voltage versus supply voltage

Seven Stage Frequency Divider

Monolithic integrated seven stage frequency divider in bipolar technique, primarily for use in electronic organs. The seven flip-flops have externally accessible inputs and outputs.

Each flip-flop changes state on application of a positive-going input pulse. The individual flip-flops can be interconnected to form a divider chain. Two flip-flop pairs are already internally series-connected as shown in Fig. 2.

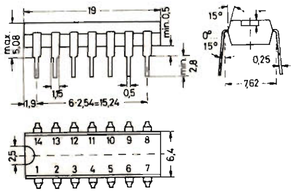
An emitter-follower is interposed between each flip-flop and the associated output pin to ensure that the output voltage is largely independent of load. Because no internal emitter resistors are provided, the emitter-follower delivers unidirectional output currents.

When used in electronic organs the frequency divider SAJ 110 may be driven by sine wave as well as square wave signals. The shape of the square wave output signal can be modified by connecting *RC* filters.

If, by means of an appropriate circuit, all inputs and outputs are brought to a potential below 1.5 V for a short time, all outputs remain in the low state.

Fig. 1:
SAJ 110 in dual in-line (Dil) plastic TO-116 package
20 A 14 according to DIN 41 866

Weight approx. 1.1 g
Dimensions in mm



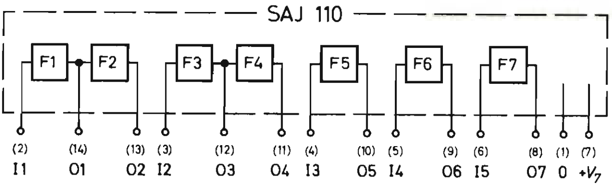


Fig. 2: Block diagram of the SAJ 110
The figures in brackets correspond to the pin numbers

All voltages are referred to pin 1.

Maximum Ratings

Supply voltage	V_7	11	V
Input voltage		see Fig. 6	
Output current per stage	I_o	5 [1])	mA
External voltage at output pins	V_{ext}	±5	V
Ambient operating temp. range	T_{amb}	−10...+60	°C
Storage temperatur range	T_S	−30...+125	°C

Characteristics per Divider Stage
for $V_7 = 9$ V, $R_L = 2.2$ kΩ, $T_{amb} = 25$ °C

Supply current (low state at output)	I	< 3	mA
Input voltage high state (see Fig. 6)	V_{IH}	6...9	V
Input voltage low state	V_{IL}	< 1	V
Output voltage low state	V_{OL}	< 0.1	V
Output voltage high state	V_{OH}	> 7.0	V
Rise time of output voltage	t_r	< 0.2	µs
Fall time of output voltage	t_f	< 0.2	µs
Input resistance (see Fig. 7)	r_i	6...9	kΩ
Output resistance low state	r_o	> 1	MΩ
Output resistance high state	r_o	200	Ω

[1]) During resetting in accordance with Figs. 4 and 8 this value may be exceeded for a time less than 0.1 ms.

Recommended Operating Conditions

Supply voltage	V_7	9	V
Max. input frequency	f_{imax}	50	kHz
Load resistance	R_L	2 . . . 20	kΩ

If the output voltage shape has to be modified for applications in electronic organs (see Fig. 3), a protective resistor $R_S = 180\ \Omega$, connected in series with the capacitor C_L, should be used. In this case the condition $R_L \gg R_S$ must be met.

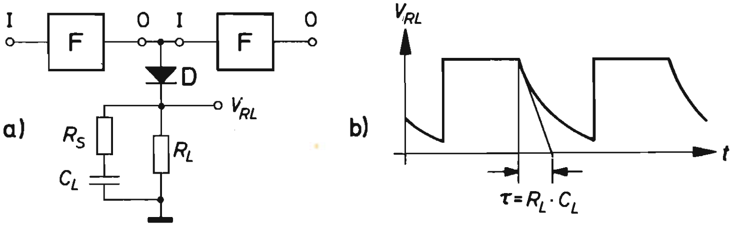


Fig. 3: Modification of square wave output voltage using *RC* networks

a) Circuit diagram, D = Decoupling diode, e. g. BA 170
b) Shape of output voltage V_{RL}

On application in counter circuits resetting may be required. This can be accomplished by bringing all outputs to a potential less than 3 V with the inputs kept at 0 V as shown in Fig. 8, or more conveniently by bringing all inputs and outputs to a potential less than 1.5 V. The active edge of the reset pulse has to be fast enough to complete the resetting within less than 0.1 ms, otherwise the device may be overloaded. Fig. 4 shows a recommended circuit for resetting.

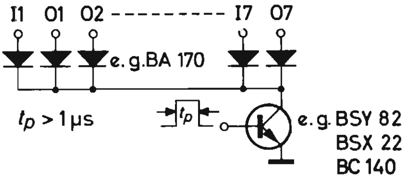


Fig. 4: Recommended reset circuit for counting applications

Fig. 5:
Output voltage versus supply voltage

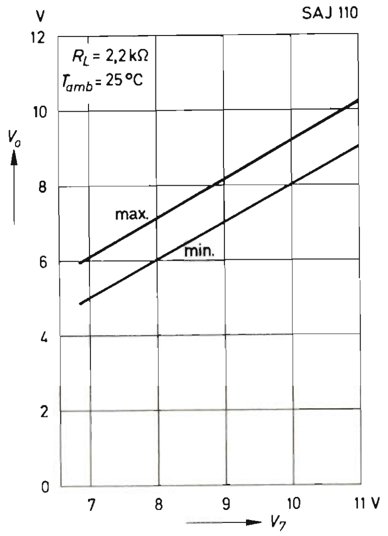


Fig. 6:
Max. admissible and min. required value of input pulses (high state) versus supply voltage

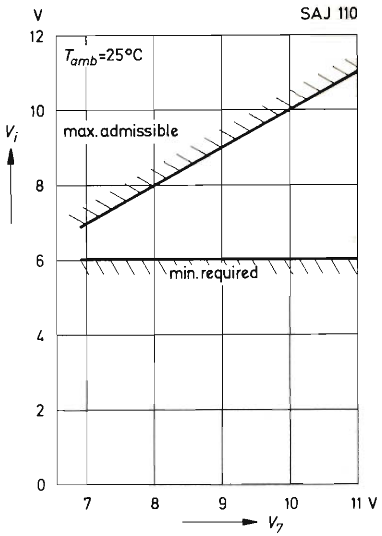


Fig. 7:
Input characteristic

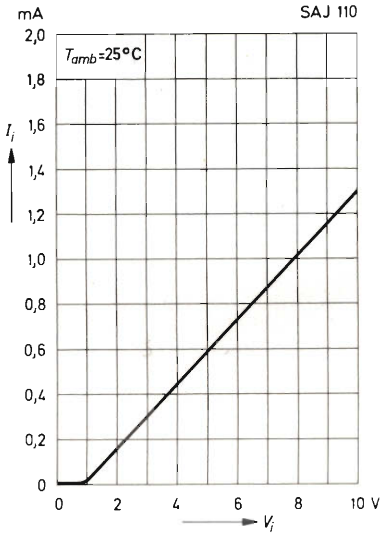
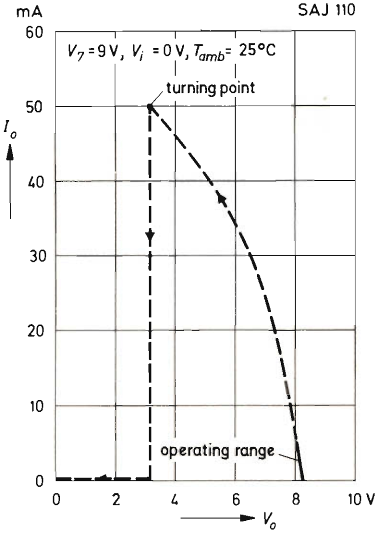


Fig. 8:
Output characteristic



Gate for Electronic Organs

Pin compatible, improved version of the TDA 0470

Monolithic integrated circuit in bipolar technique, designed primarily for use in electronic organs. The device incorporates twelve transistors, each replacing a mechanical key-contact. Thus it is possible to reduce the numerous mechanical key-contacts on conventional organs (up to ten per key) to one single contact per key.

Each tone-signal to be switched may be fed into one of the twelve emitters as a driving current. The transfer of the different signals to the common collector is effected by DC voltages. The sum of all signals will be derived at pin 14.

The additional integrated clamping diodes limit the signal voltage at each emitter when the transistors are cut off thus reducing crosstalk via the capacitances of the blocked transistors.

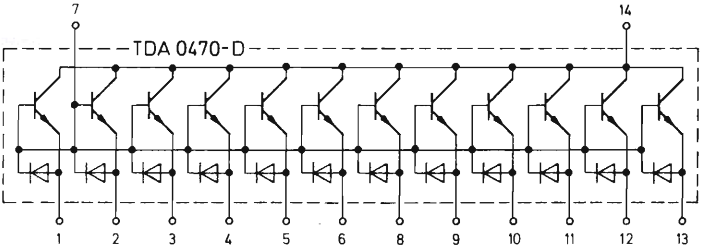
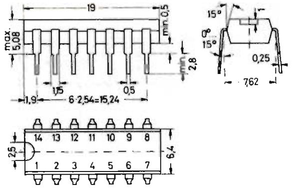


Fig. 1: Internal circuitry of the TDA 0470-D

Fig. 2:
TDA 0470-D in dual in-line (Dil) plastic TO-116 package
20 A 14 according to DIN 41 866

Weight approx. 1.1 g
Dimensions in mm



Maximum Ratings

Collector current	I_{14}	25	mA
Emitter current (per emitter)	I_E	-5	mA
Base current	I_7	25	mA
Collector emitter voltage	V_{CE0}	22	V
Power dissipation at $T_{amb} = 60\ ^\circ C$	P_{tot}	250	mW
Ambient operating temp. range	T_{amb}	$-10 \ldots +60$	°C

Characteristics at $T_{amb} = 25\ ^\circ C$
(of each stage)

DC current gain at $V_{CE} = 2$ V, $I_C = 1$ mA	h_{FE}	> 40	
Collector saturation voltage at $I_C = 1$ mA, $I_B = 0.1$ mA	$V_{CE\,sat}$	< 0.4	V
Collector emitter cutoff current at $V_{CE} = 15$ V	I_{CES}	< 30	nA
Emitter base voltage at $I_E = 1$ mA	V_{EB}	0.75	V

ICs for Other Applications

Telephone Push-Button Dialling IC

Monolithic integrated circuit in MOS technique for use in telephone sets with dialling push-buttons.

Special Features:

The off-normal output is released during the inter digital pause

Decoding by means of ROM gives flexible code

Two different dial pulse ratios optional

Two different inter digital pauses optional

The SAH 215 — Design and Operation

This circuit makes it possible to design push-button dialling telephone sets for connection to conventional telephone networks (quickstep-dialling).

The MOS circuit requires a two-phase clock generator which delivers two non-overlapping clock pulses having an amplitude of approximately − 18 V. Its power consumption can be kept to the extremely low value of less than 4 mW.

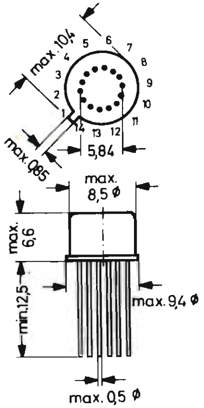


Fig. 1:
SAH 215 in metal case
≈ TO-5 with 14 leads

Weight approximately 1 g
Dimensions in mm

Pin connections

1	Case, substrate, ground
2	o. n. output
3	d. p. output
4	Reset input
5	Strobe input
6	External register control input
7	Clock *t1*
8	Clock *t2*
9	Input A
10	Input B
11	Input C
12	Input D
13	Option I
14	Option II

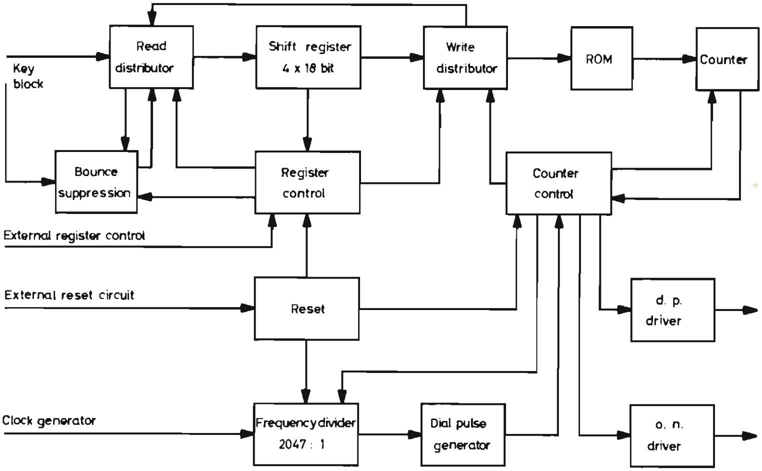


Fig. 2: Block diagram of the SAH 215

Fig. 2 shows the block diagram of the SAH 215. Four-bit data arriving from the key block are fed in parallel to the shift register via the read distributor. This register consists of four parallel individual registers of 18 bits each and serves for storing a maximum of 18 figures. A bounce-suppression circuit prevents a dialled figure from being written into the register more than once, due to contact bounce in the key block. The register control unit ensures the proper writing and reading sequence.

Through the write distributor the data are taken to a read only memory (ROM) which operates as a decoder and sets a counter in accordance with the entered figure. Through the counter control unit, the dial pulse generator transmits the number of pulses for which the counter was set to the d. p. (dial pulse) driver, maintaining the proper pulse duty factor. The counter control unit maintains the required interval between the several pulse trains and controls the o. n. driver.

The dial pulse generator frequency is derived from the clock frequency by means of a 2047:1 frequency divider. For the customary dialling frequency of 10 Hz the required clock frequency is therefore 20.47 kHz.

When applying the supply voltage to the MOS circuit, all stages of the control units have to be reset. This is achieved by a built-in reset unit which is controlled by an external circuit. The "0" → "1" slope of the reset signal must be at least 1 V/ms.

Fig. 3 shows a block diagram of the whole circuit arrangement.

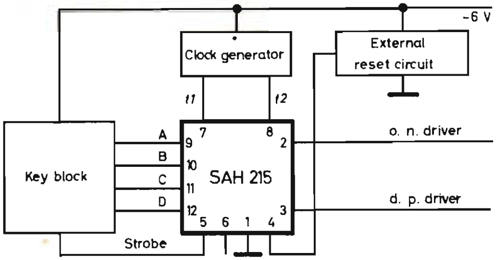


Fig. 3: Block diagram of the general layout

The SAH 215 operates with the following code:

	Figure	D	C	B	A
	1	0	0	0	0
	2	0	0	0	1
	3	0	0	1	0
	4	X	1	0	0
	5	0	1	X	1
	6	0	1	1	0
	7	1	0	0	0
	8	1	X	0	1
or	8	1	0	X	1
	9	1	0	1	0
	0	0	0	1	1

The information in this table relates to "negative logic", i. e. the more negative voltage level (Low) stands for logic "1", and the more positive voltage level (High) for logic "0". The symbol "X" may be an "0" or a "1" (see also page 12).

When using a key block in which each key is provided with two ordinary contacts and one positively controlled n. o. (non-overlapping) contact it is possible to control the integrated circuit directly. The same applies to a key block with row and column switches each of which is provided with a common positively controlled n. o. contact. The positively controlled n. o. contacts which close after the other n. o. contacts and open before the other n. o. contacts, control the strobe input 5. Key blocks of different design may be adapted by using a diode matrix. A general requirement for key blocks is that the data signals must be free from bounce prior to the strobe signal as each key is depressed.

Further possibilities of adaptation are introduced by mask variations which enable any desired four-bit code to be set, as long as the tetrades 1111 and 1110 do not occur, because they are needed for register control.

An additional facility

In normal use the terminal 6 is not loaded. This corresponds to a logic "1". If a logic "0" signal is applied to this terminal the register output is blocked and the data made to circulate in the register. In this way, up to 17 figures can be stored. By applying appropriate pulse patterns to terminal 6 individual figures or figure blocks may be recalled. The input of data is not affected by a signal being applied to terminal 6, so that the storage of figures can continue.

All voltages are referred to terminal 1.

Maximum Ratings

Voltages, clock pulse 1, clock pulse 2	V_7, V_8	– 30 . . . + 0.3	V
Input voltages Inputs 4, 5, 9, 10, 11 and 12	V_{in}	– 30 . . . + 0.3	V
Output current	I_2, I_3	– 5	mA
Ambient temperature range	T_{amb}	– 40 . . . + 70	°C

Recommended Operating Conditions

Clock pulse voltages	V_{7M}, V_{8M}	– 18	V
Clock frequency	f_t	20 (10 . . . 50)	kHz
Duration of clock pulses	t_t	> 5	µs
Time interval between clock pulses 1 and 2	t_a	> 3	µs
Reset voltage	$-V_4$	< 3	V
Duration of normalisation pulse	t_4	> 1	ms
Strobe input time (free from bounce)	t_E	> 17	ms
Bounce/strobe pulse spacing	t_B	< 7	ms

Characteristics at $V_{7M} = V_{8M} = -18$ V, $T_{amb} = 25$ °C

Input voltages Inputs 4, 5, 9, 10, 11 and 12			
Logic "0"	V_{in}	Terminal open	
Logic "1"	V_{in}	– 6 (– 5 . . . – 12) V	
Input 6			
Logic "0"	V_{in}	0 . . . – 3	V
Logic "1"	V_{in}	Terminal open	
Input cutoff current at $V_{in} = -12$ V	$-I_R$	5	µA
Output frequency	f_{out}	f_t/2047	
Power consumption	P_{tot}	< 4	mW
Capacitance of clock inputs	C_7, C_8	< 150	pF

The time t_z of the inter digital pause at f_t = 20.47 kHz and the output pulse duty factor t_p/T are changeable by different circuiting of the Option I and Option II pins.

Option I and Option II open	t_p/T	0.66	
	t_z	433	ms
Option I open, Option II to ground	t_p/T	0.62	
	t_z	438	ms
Option I to ground, Option II open	t_p/T	0.66	
	t_z	833	ms
Option I and Option II to ground	t_p/T	0.62	
	t_z	838	ms

Delay Line for Analogue Signals

Monolithic integrated circuit in MOS technology for the delay of analogue signals in the frequency range up to 250 kHz. It ist designed according to the principle of the bucket circuit and comprises 185 series-connected field effect transistors and 185 integrated capacitors.

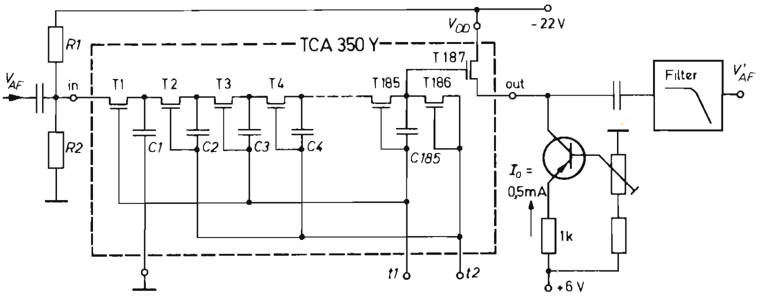
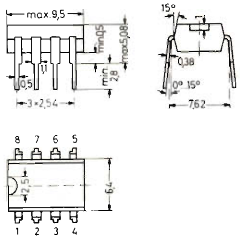


Fig. 1: Internal circuitry and test circuit of the TCA 350 Y with external components

Fig. 2:
TCA 350 Y in plastic package
20 A 8 according to DIN 41 866

Weight approx. 0.5 g
Dimensions in mm



Pin connections

1 Leave vacant
2 Clock input *t2*
3 Delay line input
4 Ground, 0
5 Clock input *t1*
6 Delay line output
7 V_{DD}
8 NC

All voltages are referred to ground (pin 4)

Maximum Ratings

Drain voltage	V_{DD}	– 30 . . . + 0.3	V
Input voltage	V_{in}	– 30 . . . + 0.3	V
Clock pulse voltages	V_{t1}, V_{t2}	– 30 . . . + 0.3	V
Output current	I_o	– 5	mA
Storage temperature range	T_S	– 40 . . . + 100	°C

Recommended Operating Conditions

Drain voltage	V_{DD}	– 22 (– 20 . . . – 24)	V
Clock pulse voltage (see Fig. 7) high state	V_{tH}	– 1 . . . + 0.3	V
low state	V_{tL}	– 18 (– 17.5 . . . – 20)	V
Clock frequency (see Fig. 5) when $f_t > 2\ f_{AFmax}$	$f_t = \frac{1}{T_t}$	40 (10 . . . 500)	kHz
Clock pulse duration	t_1, t_2	$>$ 0.8	µs
Interval between two clock pulses	t_{1p}, t_{2p}	$>$ 0 (not overlapping)	
Signal pulse duty factor (see Fig. 8)	$\frac{t_1 + t_{1p}}{T_t}$	0.1 . . . 0.9 [1])	
Rise and fall time of the clock pulses	t_r, t_f	0.05 . . . 10	µs
Input bias voltage	V_{in}	– 8 (– 7.5 . . . – 8.5)	V
Impedance of bias source at the input	$\frac{R_1 \cdot R_2}{R_1 + R_2}$	$<$ 20	kΩ
Input signal amplitude (peak-to-peak, see Fig. 10)	V_{AFpp}	3 (0 . . . 6)	V
Input impedance of the filter at output	R_{inF}	$>$ 20	kΩ
Output DC current (current of the constant current source see Fig. 11)	I_o	0.5 . . . 1.5[2])	mA
Ambient operating temp. range	T_{amb}	– 20 . . . + 60	°C

[1]) The output signal is proportional $\frac{t_1 + t_{1p}}{T}$, because during the time $t_1 + t_{1p}$ the AF signal appears at the output.

[2]) If the filter input impedance R_{IF} exceeds 1 MΩ, the constant current source at the output may be replaced by a resistor $R_L > 10$ kΩ (see Fig. 12).

Characteristics

at $V_{DD} = -22$ V, $V_{in} = -8$ V, $V_{AFpp} = 6$ V, $f_{AF} = 400$ Hz, $V_{fH} = 0$, $V_{fL} = -18$ V, $f_f = 40$ kHz, $t_1/T_f = t_2/T_f = 0.48$, $t_r = t_f = 2$ µs, I_o = 0.5 mA, $T_{amb} = 25$ °C in the circuit Fig. 1 which includes the Butterworth filter at the output. The latter has a cutoff frequency of 8 kHz, an input impedance of 43 kΩ and an attenuation of 110 dB at kHz. These test conditions apply equally to Figs. 3 . . . 12.

Delay time ($\tau = \frac{184}{2 \cdot f_f}$)	τ	2.3	ms
Attenuation [1])	a	8.5 (< 10)	dB
Distortion factor	k	0.5 (< 3)	%
Noise voltage, peak-to-peak (see Fig. 6)	V_{Npp}	1.2 (< 2)	mV
Noise voltage, RMS value (see Fig. 6)	$V_{N\,RMS}$	0.2 (< 0.35)	mV
Clock input capacitances	C_f	150	pF

[1]) In the test circuit the AF signal appears at the output only for the duration $t_1 + t_{1p} = T/2$. This amounts to a 6 dB attenuation. Only the residual 2.5 . . . 4 dB of the above quoted attenuation can be ascribed to the delay line.

Design and Operation Mode

Fig. 1 shows the circuit diagram of the TCA 350 Y and the external circuit components.

The output transistor T 187 requires a drain voltage of – 22 V from which the necessary input bias of – 8 V is produced by a potential divider. Connected to the source terminal of the output transistor T 187, which operates as a source follower, is a 0.5 mA constant current source which acts as a load resistance and caters for voltage variations from + 5 V to – 22 V at the output of the TCA 350 Y. This ensures distortion-free transmission of the two bands of the output signal (see Fig. 3).

Fig. 4 illustrates the time relationship between clock signal and output signal as scaled by the clock frequency. The information contained in the output signal appears during the onset of clock pulse t_1 and is maintained up to the onset of clock pulse t_2. During t_1 the input information is scanned, i. e. the capacitor *C1* absorbs the information via the turned-on transistor T1. Every subsequent clock pulse (t_1 as well as t_2) shifts this information into the next capacitor of the chain. With the 185th pulse (of which 93 pulses are t_1 and 92 pulses t_2) the information reaches the last capacitor of the chain, i. e. *C185*, and, after amplification, becomes available via the source-follower T187 at the output of the TCA 350 Y. As is apparent from Fig. 4, the information is preserved up to the onset of t_2, although the signal voltage is raised by about 14 V after the expiry of t_1.

In this way the lower signal band is produced during t_1, and the upper signal band during t_{1p}. Which proportion of the intelligence is contained in the lower, and which in the upper signal band depends upon the ratio of the clock pulse duration t_1 to the clock pulse interval t_{1p}. Thus, if $t_{1p} = 0$ information is transmitted exclusively in the lower signal band.

The delay time of the bucket brigade circuit TCA 350 Y is calculated by using the following equation:

$$\tau = \frac{n}{2 \cdot f_t} = \frac{184}{2 \cdot f_t}$$

wherein n is the number of buckets in the chain (in the present case 184 because capacitor *C1* does not contribute to the delay time).

The lowpass connected to the output of the TCA 350 Y filters the delayed signal V'_{AF} from the output signal of the TCA 350 Y which contains the clock voltage.

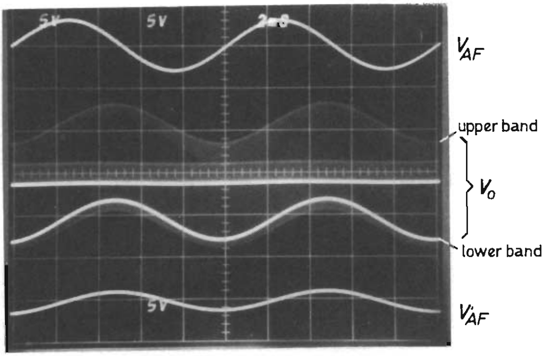


Fig. 3: Input and output voltages of the circuit shown in Fig. 1

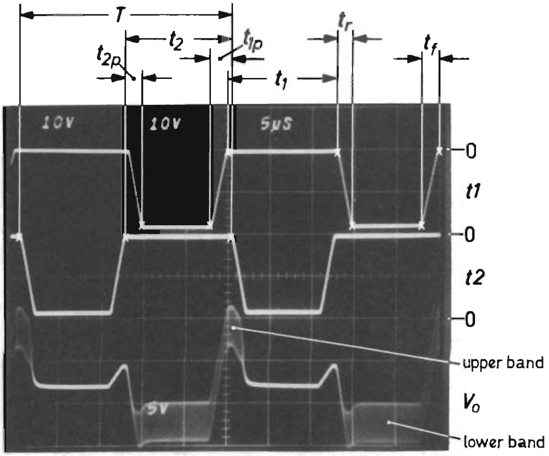


Fig. 4: Output voltage and clock voltages of the circuit shown in Fig. 1

Fig. 5:
Distortion factor versus clock frequency

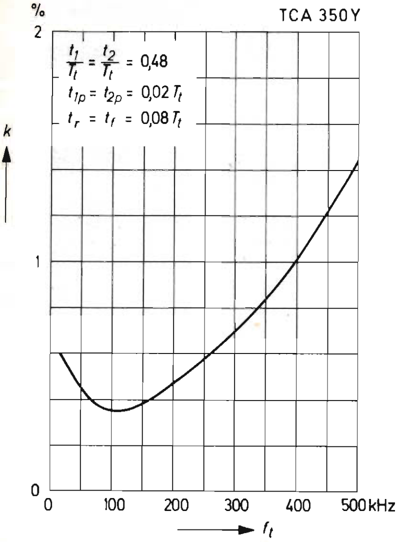


Fig. 6:
Noise voltage versus clock frequency

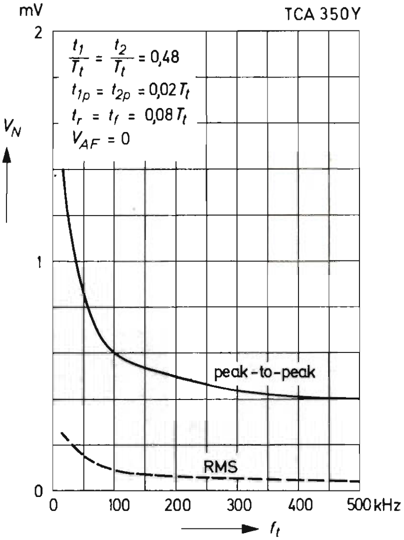


Fig. 7:
Distortion factor versus clock amplitude

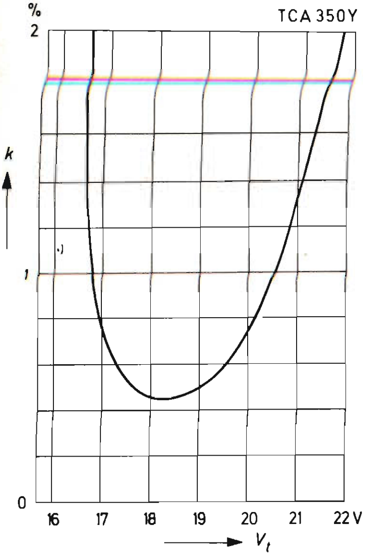


Fig. 8:
Distortion factor versus pulse duty factor of the clock signal

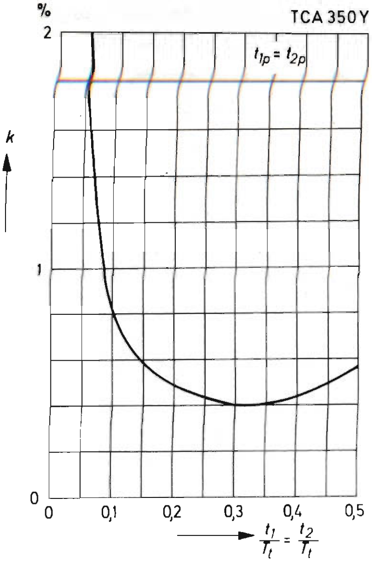


Fig. 9:
Distortion factor versus
signal pulse duty factor

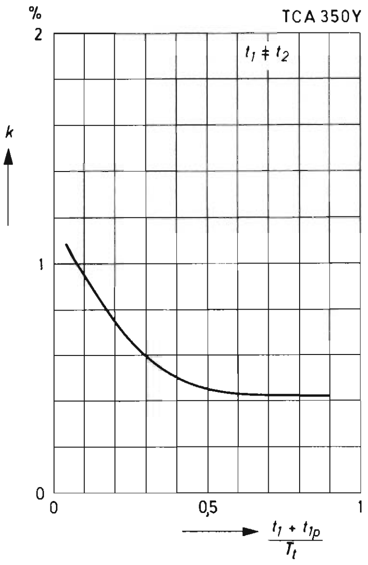


Fig. 10:
Distortion factor versus
signal amplitude at input

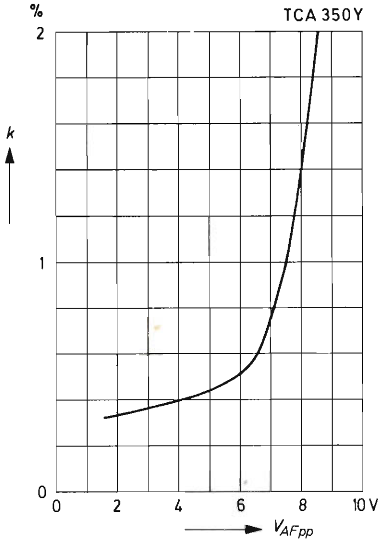


Fig. 11:
Distortion factor
versus current of
constant current source

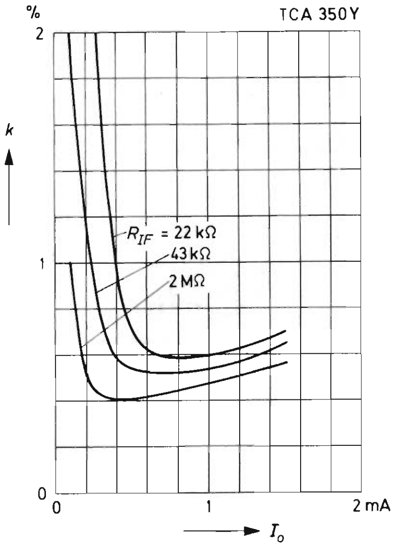
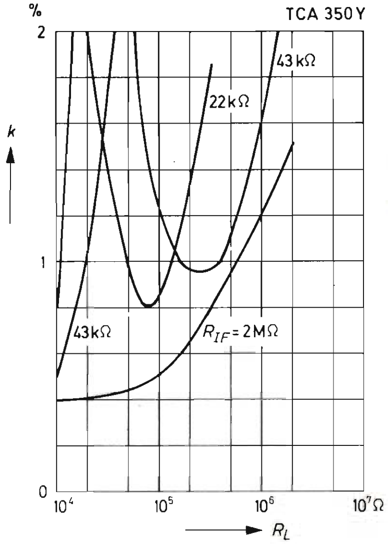


Fig. 12:
Distortion factor versus
ohmic load resistance
at output



Duplex RF Delay Line

Monolithic integrated MOS circuit for the variable delay of video and RF signals. The TCA 380 operates on the bucket brigade principle. The "buckets" contained in the circuit are 2 x 190 small integrated MOS capacitors. The signal is advanced from one capacitor to the next at the rhythm of the clock frequency and is thus delayed. By varying the clock frequency the time delay can be altered. Being a duplex delay line, the TCA 380 comprises two bucket brigade circuits whose inputs and outputs are connected in parallel. The clock signal is applied to the two bucket brigades in antiphase. This type of circuit offers the advantage that attenuation and signal-to-noise ratio are better by 6 dB than in a single bucket brigade. Moreover, the duplex configuration permit of a higher upper-end limit frequency. Whereas with a simple bucket brigade the high-end limit frequency is equal to half the clock frequency, the high-end limit frequency in the case of the duplex circuit is theoretically equal to the clock frequency. Fig. 1 is a diagram of the internal TCA 380 circuit. $V_1 \ldots V_4$ are the attenuation-compensating stages mentioned overleaf.

The attainable signal delay τ depends, according to the following equation, upon the number of stages n and upon the clock frequency f_t:

$$\tau = \frac{n}{2f_t} = \frac{190}{2f_t}$$

By varying the clock frequency between the values $f_{t\,min}$ and $f_{t\,max}$, we obtain the differential delay

$$\Delta\tau = \frac{n}{2} \cdot \left(\frac{1}{f_{t\,min}} - \frac{1}{f_{t\,max}}\right)$$

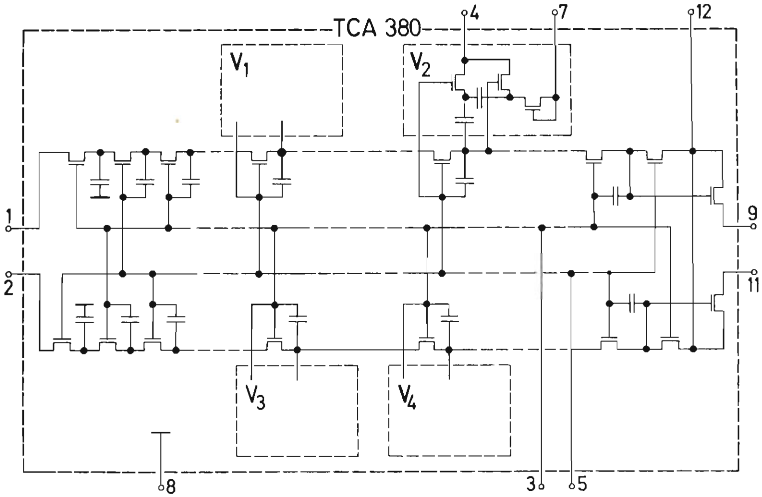


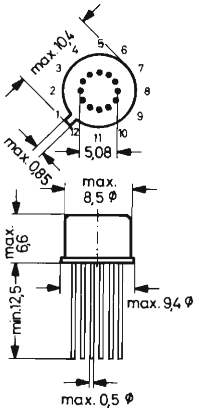
Fig. 1: Internal circuit of the TCA 380 (diagrammatic)

By means of likewise integrated attenuation-compensating stages, signal components of a higher frequency can be emphasised. This enables the frequency response of the delay line to be equalised by selecting the compensating voltage. If the clock frequency varies, the attenuation-compensating voltage may be varied in dependence on frequency.

It is advisable to let a lowpass filter precede the delay line whose upper cutoff frequency is lower than the smallest clock frequency $f_{t\,min}$. Similarly, a lowpass filter should be included after the delay line which suppresses the clock signal superimposed on the intelligence signal.

Fig. 2:
TCA 380 in TO-73 metal case
similar to TO-5 with 12 leads

Weight approximately 1 g
Dimensions in mm



Pin connections

1	Input 1
2	Input 2
3	Clock *t1*
4	Compensation V_{comp}
5	Clock *t2*
6	leave vacant!
7	Supply voltage (compensation)
8	Ground, 0, case, substrate
9	Output 1
10	leave vacant!
11	Output 2
12	Supply voltage

All voltages are referred to pin 8.

Maximum Ratings

Supply voltage	V_7, V_{12}	0 . . . 30	V
Input DC voltages	V_1, V_2	0 . . . 30	V
Input signal voltage with 10 kΩ limiting resistor between signal source and input	V_{1pp}, V_{2pp}	10	V
Clock voltages	V_3, V_5	0 . . . 30	V
Attenuation compensating voltage	V_{comp}	0 . . . 30	V
Output rating	Pins 9 and 11 are short-circuit proof with respect to each pin		
Ambient operating temp. range	T_{amb}	0 . . . 60	°C
Storage temperature range	T_S	–20 . . . +80	°C

Recommended Operating Conditions

Supply voltages	V_7, V_{12}	18 . . . 24	V
Compensation voltage	V_{comp}	8 . . . 10	V
Input DC voltages	V_1, V_2	$(0.4 \ldots 0.7) \cdot V_{12}$	
Output voltages	V_{9pp}, V_{11pp}	1.5	V
Clock voltages	$V_{3H} = V_{5H}$	$< V_{12}$	
Shape of clock signal	see diagrams 4 and 5		

Characteristics at $V_{3H} = V_{5H} = V_7 = V_{12} = 20$ V, $T_{amb} = 25$ °C, clock signal corresponding to diagrams 4 and 5 in the test circuit of Fig. 3

Number of capacitors of one bucket brigade	n	190	
Gain at $f_s = 100$ kHz, $f_t = 5$ MHz	$G_{100\,kHz}$	–9 . . . +3	dB
Loss of gain at $f_s = 3$ MHz, $f_t = 5$ MHz, referred to $f_s = 100$ kHz	$\frac{G_{100\,kHz}}{G_{3\,MHz}}$	< 20	dB
Loss of gain at $f_s = 5$ Hz, $f_t = 5$ MHz, referred to $f_s = 100$ kHz	$\frac{G_{100\,kHz}}{G_{5\,Hz}}$	< 6	dB
Signal-to-noise ratio at $f_s = 3$ MHz, $f_t = 5$ MHz and noise bandwidth 0 . . . 3 MHz	$\frac{V_{out}}{V_n}$	> 25	dB
Distortion factor at $f_s = 20$ kHz, $f_t = 5$ MHz, $V_{out\,pp} = 1.2$ V	k	< 5	%
Crosstalk attenuation between input and output at $f_t = 5$ MHz	a	> 30	dB
Ratio of the output signal to the clock frequency dependent level fluctuation with 25 Hz modulation of the clock frequency between 3.5 MHz and 5.5 MHz at $V_{out\,pp} = 1.5$ V	$\frac{V_{out}}{\Delta V_{out}}$	> 30	dB
Difference of the delay times when operating with a clock frequency of 3.5 or 5.5 MHz	$\Delta\tau$	10	µs

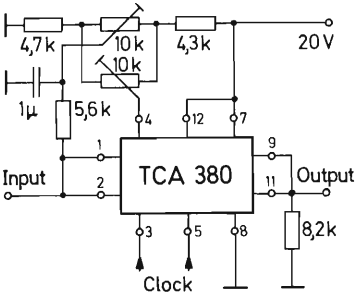


Fig. 3: Test circuit

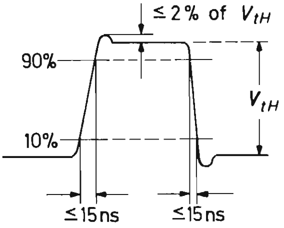


Fig. 4: Required waveform of clock signal

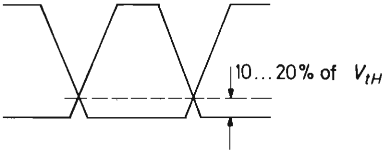


Fig. 5: Admissible overlapping of the clock pulse slope at f_t = 4 MHz

Voltage Stabilizers for 5 . . . 24 V

Monolithic integrated voltage stabilizers in bipolar technology for stabilizing voltages of 5 V to 24 V (± 5 %), with load currents of 500 mA to 200 mA, equipped with overload protection by current limiting with a reversing characteristic. When the excess load is removed the stabilized voltage returns by itself. Low drift, high stabilizing factor and low consumption in the non-operative condition are further features of these modern components.

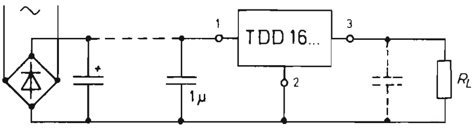
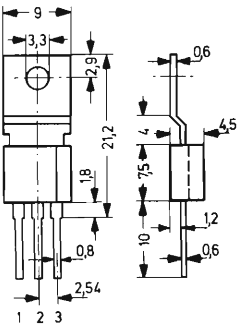


Fig. 1: Connection diagram of the voltage stabilizers TDD 16 . . and application circuit

Fig. 2:
Plastic case similar to 34 A 3
Pin 2 (ground) is connected to the cooling fin.

Weight approximately 1.5 g
Dimensions in mm



All voltages are referred to pin 2.

Maximum Ratings

Input voltage			
TDD 1605 . . . TDD 1618	V_I	35[1])	V
TDD 1624	V_I	40	V
Temperature of chip	T_j	125	°C
Storage temperature range	T_S	– 20 . . . +125	°C

[1]) Upon request all types are available with an admissible input voltage of 40 V.

Characteristics at $T_C = 25\ °C$ and $V_I = (V_3 + 5\ V)$

Type	Stabilized voltage tol. ± 5 % V_3 V	Maximum load current $-I_{3\ op}$ mA	Onset of current limiting $-I_{3\ max}$ mA	Output resistance $\Delta V_3/\Delta I_3$ mΩ
TDD 1605	5	500	1000	75
TDD 1606	6	500	1000	75
TDD 1608	8.5	500	1000	75
TDD 1610	10	500	1000	100
TDD 1612	12	500	1000	100
TDD 1615	15	400	800	150
TDD 1618	18	300	600	150
TDD 1624	24	200	400	200

Voltage tolerance at $-I_3 = 10$ mA	ΔV_3	± 5	%
Stabilizing factor at $f = 100$ Hz	$\Delta V_I/\Delta V_3$	> 200	
Temperature dependence of the output voltage	$\frac{\Delta V_3}{\Delta T_C \cdot V_3}$	10^{-4}	1/°C
No-load current consumption at $I_3 = 0$	I_{1r}	7	mA
Short-circuit current	$-I_{3\ short}$	50	mA
required longitudinal voltage at $-I_{3\ op}$	$V_{1/3}$	> 2.5	V
Thermal resistance Chip – cooling fin	R_{thC}	10	°C/W
Chip – ambient air	R_{thA}	70	°C/W

The power to be dissipated can be calculated by the equation

$$P_{tot} = V_I \cdot I_{1r} + (V_I - V_3) \cdot I_3$$

From the maximum possible power the thermal resistance of the required cooling surface or radiator has to be calculated by the equation

$$R_{thS} = \frac{T_j - T_{amb}}{P_{tot}} - R_{thC}.$$

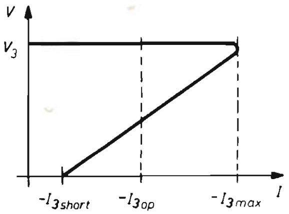


Fig. 3: Output characteristic

Exposurementer-IC

Monolithic integrated circuit in bipolar technology, for application in simple photographic cameras with fixed exposure time.

The UAA 210 comprises a window comparator with close tolerances and a 10 mA constant-current source supplying a light-emitting diode. Fig. 1 shows the application circuit. The photo-conductive element R_F, which is fitted beside the camera objective, measures the light impinging upon the camera and the light-emitting diode is extinguished when the correct stop has been set. Otherwise the stop, as well as a slide provided in front of the photoconductive cell and mechanically coupled to the stop will have to be displaced until the light-emitting diode is extinguished.

The characteristic of the window comparator (Fig. 4) is chosen in such a way that that the indicator lamp is extinguished for a range comprising one light value, i. e. the maximum exposure error can only amount to one light value. Below a predetermined battery voltage, the light-emitting diode receives no current, which amounts to a voltage deficiency check within the UAA 210.

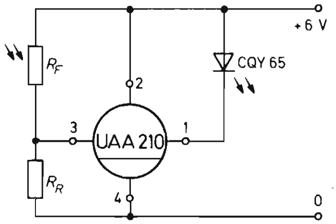
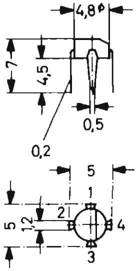


Fig. 1: Operating circuit for the UAA 210

Fig. 2:
UAA 210 in plastic package
50 B 4 according to DIN 41 867

Weight approximately 0.1 g
Dimensions in mm



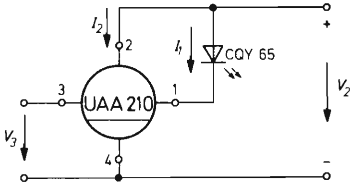


Fig. 3: Circuit for testing the characteristics

All voltages are referred to pin 4.

Definitions

I_2:	Current consumption of the UAA 210 at $R_F = 0$
R_B:	Internal resistance of the battery for which no functional failure occurs within the supply voltage range (V_{2A} + 0.2 V) to 6 V.
V_{2A}:	The supply voltage cut out level is determined by the fact that, with T_{amb} = 23 . . . 25 °C and X = 0.33 or X = 0.75, the output current I_1 = 10 μA.
X:	X is the symbol for the voltage ratio V_3/V_2.

Maximum Ratings

Supply voltage	V_1	6.5	V
	V_2	6.5	V
	V_3	6.5	V
Ambient temperature range	T_{amb}	– 25 . . . +70	°C
Storage temperature range	T_S	– 25 . . . +125	°C

Recommended Operating Conditions

Supply voltage (EMF of battery)	V_2	6	V
Internal resistance of battery	R_B	< 40	Ω
Resistance of the photoconductive cell	R_F	> 100	Ω
Ambient operating temperature range	T_{amb}	– 18 . . . +50	°C

Conditions for Testing the Characteristics

Condition 1: Supply voltage (± 1 %)	V_2	5	V
Ambient temperature range	T_{amb}	23 . . . 25	°C
Condition 2: Supply voltage range	V_2	(V_{2A} + 0.2 V) . . . 6 V	
Ambient temperature range	T_{amb}	23 . . . 25	°C

Condition 3:
Supply voltage range

at $T_{amb} = -18\ °C$	V_2	$(V_{2A} + 0.6\ V) \ldots 6\ V$
at $T_{amb} = +50\ °C$	V_2	$V_{2A} \ldots 6\ V$

Characteristics for the test circuit of Fig. 3, at $V_2 = 5$ V, $T_{amb} = 25\ °C$, unless otherwise specified

Supply voltage cut out level		V_{2A}	< 3.5		V
Input current at $V_3 = 5$ V		I_3	< 2		µA
		Cond. 1	Cond. 2	Cond. 3	
Current consumption	I_2	< 5	< 6	< 6	mA
Output current at $X = 1$	I_1	7.5 . . . 12.5	7.5 . . . 12.5	6 . . . 14	mA
Voltage ratios, see also Fig. 4					
at $I_1 > 4$ mA	X_u	0.508	0.504	0.500	
at $I_1 < 4$ mA	X'_u	0.532	0.536	0.540	
at $I_1 < 10$ µA	X''_u	0.538	0.544	0.550	
at $I_1 < 10$ µA	X''_o	0.676	0.670	0.664	
at $I_1 < 4$ mA	X'_o	0.682	0.678	0.674	
at $I_1 > 4$ mA	X_o	0.706	0.710	0.714	

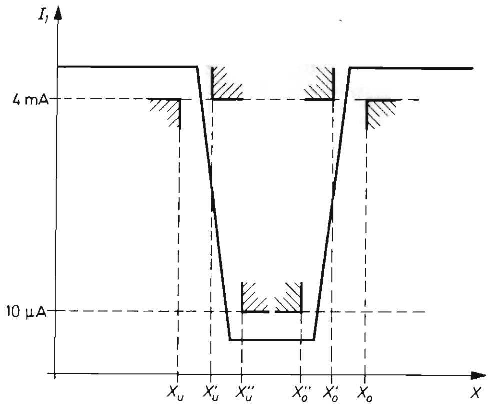


Fig. 4: Output current versus voltage ratio

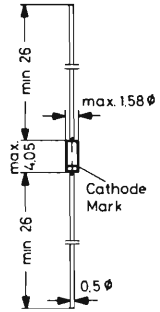
ZTE 1,5 . . . ZTE 5,1

Silicon Stabilizer Diodes

Monolithic integrated analog circuits, designed for small power stabilizer and limitation circuits, providing low dynamic resistance and high-quality stabilization performance as well as low noise. In the reverse direction, these devices show the behaviour of forward-biased silicon diodes.

The end of the ZTE device marked with the cathode ring is to be connected:
ZTE 1.5 and ZTE 2 to the negative pole of the supply voltage
ZTE 2.4   ZTE 5.1 to the positive pole of the supply voltage

Glass case JEDEC DO-35
54 A 2 according to DIN 41 880
Weight approximately 0.13 g
Dimensions in mm



Maximum Ratings

Operating current	see table on next page			
Inverse current	I_F	100		mA
Power dissipation at $T_{amb} = 25$ °C	P_{tot}	350 [1])		mW
Junction temperature	T_j	150		°C
Storage temperature range	T_S	– 55	+150	°C

Characteristics at $T_{amb} = 25$ °C

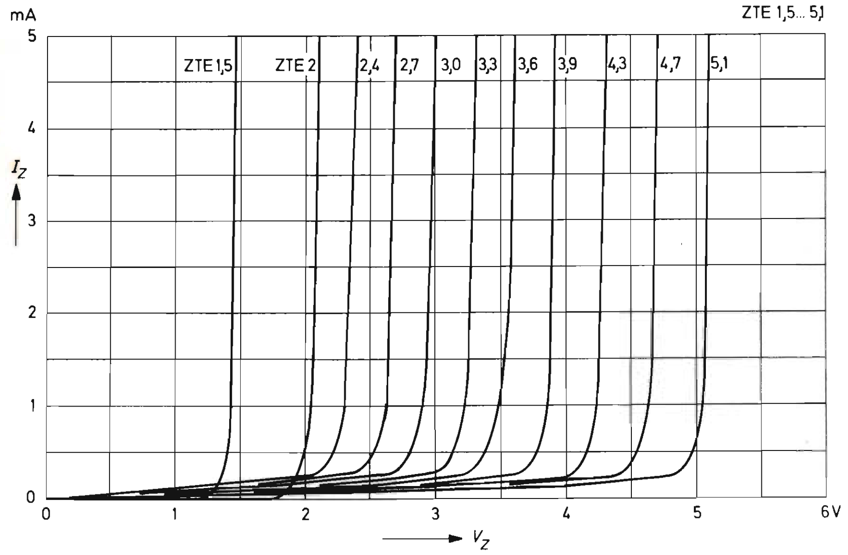
Forward voltage at $I_F = 10$ mA	V_F	< 1 1	V
Temperature coefficient of the stabilized voltage at $I_Z = 5$ mA			
ZTE 1.5 and **ZTE 2**	α_{VZ}	– 26	10^{-4}/°C
ZTE 2.4 . . . ZTE 5.1	α_{VZ}	– 34	10^{-4}/°C
Thermal resistance Junction to ambient air	R_{thA}	< 0.4 [1])	°C/mW

[1]) Valid provided that the leads are kept at ambient temperature at a distance of 8 mm from case

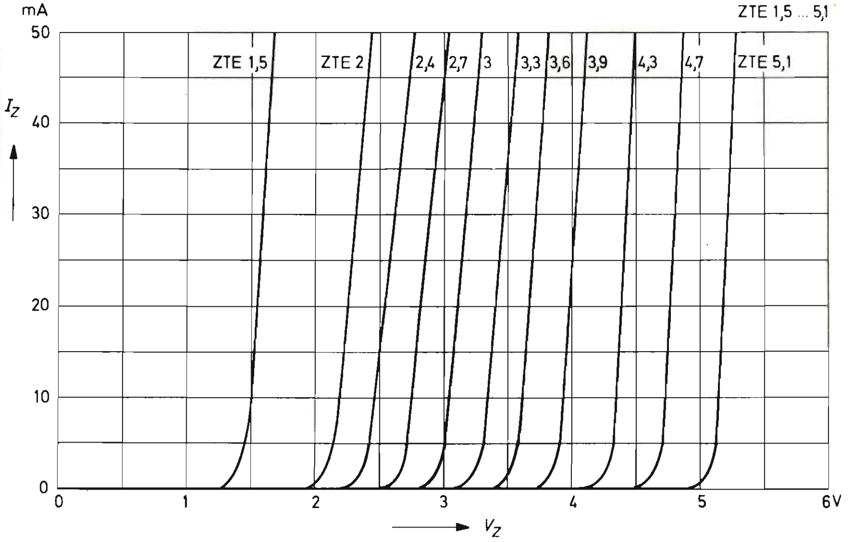
Type	Operating voltage at I_Z = 5 mA V_Z V	Dynamic resistance at I_Z = 5 mA r_{zj} Ω	permissible operating current at T_{amb} = 25 °C [1]) I_Z max. mA
ZTE 1,5	1.35 . . . 1.55	13 (< 20)	120
ZTE 2	2.0 . . . 2.3	18 (< 30)	120
ZTE 2,4	2.2 . . . 2.56	14 (< 20)	120
ZTE 2,7	2.5 . . . 2.9	15 (< 20)	105
ZTE 3	2.8 . . . 3.2	15 (< 20)	95
ZTE 3,3	3.1 . . . 3.5	16 (< 20)	90
ZTE 3,6	3.4 . . . 3.8	16 (< 25)	80
ZTE 3,9	3.7 . . . 4.1	17 (< 25)	75
ZTE 4,3	4.0 . . . 4.6	17 (< 25)	65
ZTE 4,7	4.4 . . . 5.0	18 (< 25)	60
ZTE 5,1	4.8 . . . 5.4	18 (< 25)	55

[1]) Valid provided that the leads are kept at ambient temperature at a distance of 8 mm from case.

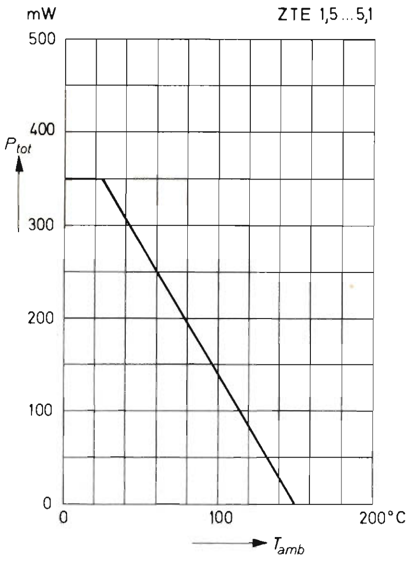
Breakdown characteristics
at T_j = constant (pulsed)



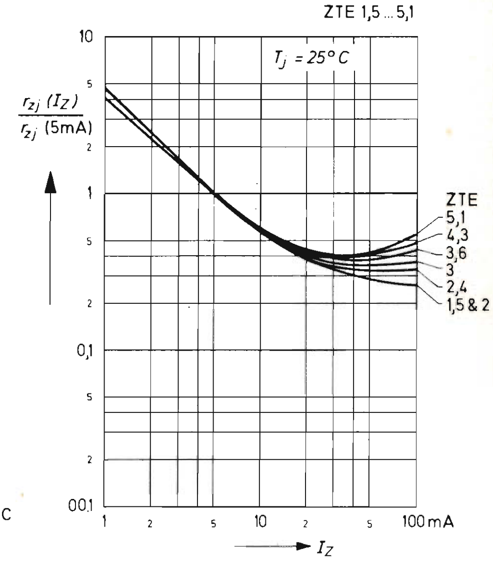
Breakdown charakteristics
at T_j = constant (pulsed)



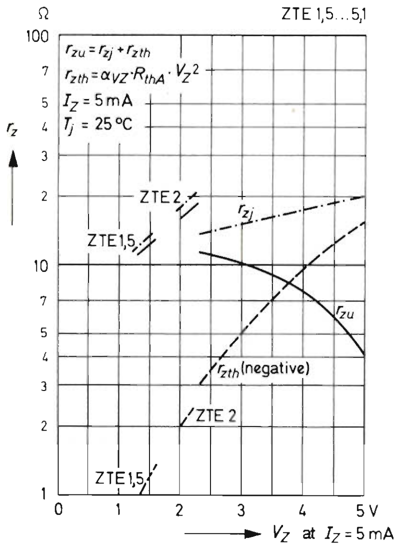
Admissible power dissipation versus ambient temperature
(see note [1]) on page 181)



Dynamic resistance versus operating current, normalised



Dynamic resistance versus operating voltage



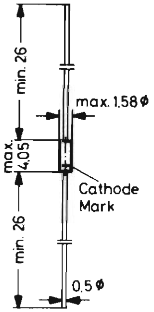
ZTK 6,8 . . . ZTK 33 (≈ TAA 550)

Temperature-Compensated Stabilizing Circuits
feature extremely short thermal run-in time

Monolithic linear integrated circuits producing an extremely constant temperature-compensated voltage, particularly suitable for stabilizing the tuning voltage in radio and TV tuners employing voltage variable capacitance diodes.

Glass case JEDEC DO-35
54 A 2 according to DIN 41 880

Weight approx. 0.13 g
Dimensions in mm



Type	Operating voltage at $I_Z = 5$ mA V_Z V	Dynamic resistance at $I_Z = 5$ mA r_{zj} Ω	maximum operating current[1]) at $T_{amb} = 45$ °C I_Z mA
ZTK 6,8	6,4 . . . 7.1	10 (< 25)	36
ZTK 9	9 . . . 10	10 (< 25)	27
ZTK 11	10 . . . 12	10 (< 25)	19
ZTK 18	16 . . . 20	11 (< 25)	13
ZTK 22	20 . . . 24	11 (< 25)	10
ZTK 27	24 . . . 30	12 (< 25)	8
ZTK 33 (≈ TAA 550)	30 . . . 36	12 (< 25)	7

admissible junction temperature	T_j	150	°C
admissible storage temp. range	T_S	− 20 . . . + 150	°C
Temperature coefficient of the operating voltage at $I_Z = 5$ mA ± 0.5 mA in the range of $T_{amb} = 20 \ldots 60$ °C	α_{VZ}	−2 (−10 . . . +5) [1])	10^{-5}/°C
Thermal run-in time	t_{th}	20 [2])	s
Thermal resistance Junction to ambient air	R_{thA}	< 0.4 [1])	°C/mW

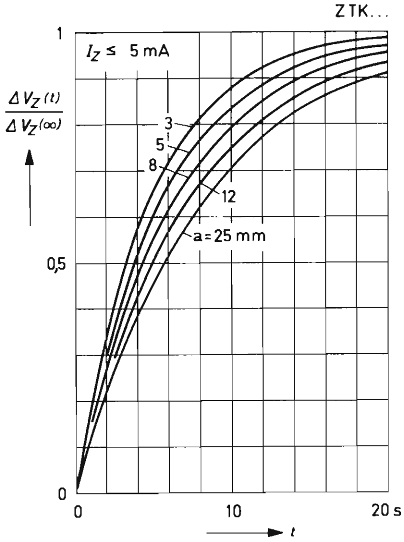
[1]) Valid provided that leads are kept at ambient temperature at a distance of 8 mm from the case.

[2]) At the end of this time ΔV_Z has reached 90 % of its final value $\Delta V_{Z\,max}$.
$\Delta V_{Z\,max} = | V_Z(\alpha) - V_Z(0) |$

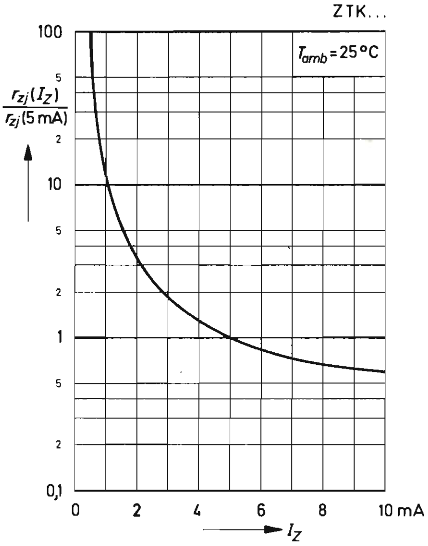
where $V_Z(0) = V_Z$ in the instant of turn-on

and $V_Z(\alpha) = V_Z$ at thermal equilibrium.

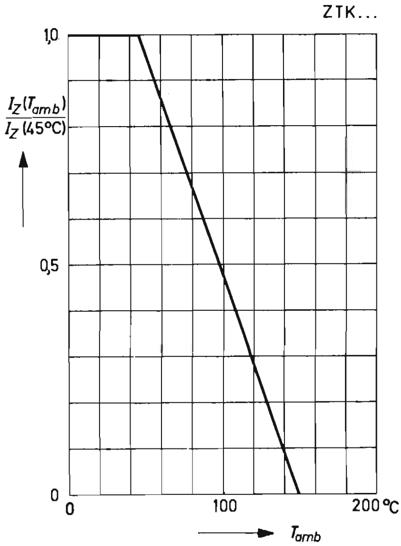
Time dependence of ΔV_Z after turn-on for different distances between case and point of ambient temperature on the leads



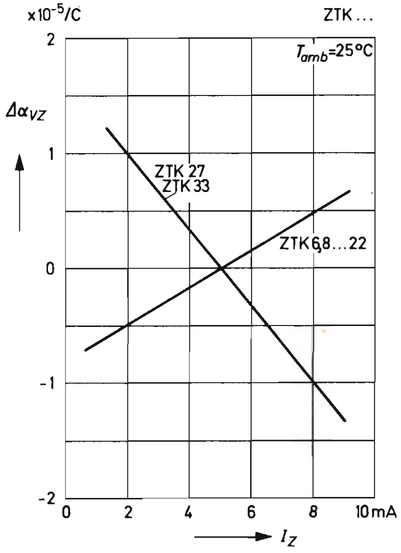
Dynamic resistance versus operating current



Permissible operating current versus ambient temperature
(see note [1]) on previous page)



Change of temperature coefficient versus operating current



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